HEWLETT PACKARD

INSTALLATION AND SERVICE MANUAL

13037D DISC CONTROLLER

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IMPORTANT NOTICE

This manual applies to the 13037D Disc Controller. Earlier 13037A, 13037B, and 13037C Disc Controllers are documented in Installation and Service Manual, part no. 13037-90006.

OPTIONS COVERED

This manual covers options 015 and 102 as well as the standard HP 13037D Disc Controller.

FOR U.S.A. ONLY

The Federal Communications Commission (in 47 CFR 15.818) has specified that the following notice be brought to the attention of the users of this product.

FEDERAL COMMUNICATIONS COMMISSION
RADIO FREQUENCY INTERFERENCE
STATEMENT

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

HEWLETT-PACKARD COMPANY
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PRINTING HISTORY

New editions incorporate all update material since the previous edition. Updating Supplements, which are issued between editions, contain additional and revised information to be incorporated into the manual by the user. The date on the title page changes only when a new edition is published.

First Printing ..... SEP 1983

NOTICE

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SAFETY CONSIDERATIONS

KEEP WITH MANUAL

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

To install or remove a fuse, first disconnect the power cord from the device. Then, using a small screwdriver, turn the fuseholder cap counterclockwise until the cap releases. Install the proper fuse in the cap — either end of the fuse can be installed in the cap. Next, install the fuse and fuseholder cap in the fuseholder by pressing the cap inwards and then turning it clockwise until it locks in place.

GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION

1-2. This installation and service manual covers general information, installation, an instruction set, theory of operation, preventive maintenance, adjustments, troubleshooting, replacement procedures, and a list of field replaceable parts for the disc controller (figure 1-1).

a. SECTION I, GENERAL INFORMATION. Provides a general description, identification, supporting documentation, and other basic information.

b. SECTION II, INSTALLATION. Provides information relative to unpacking and inspection, power requirements, mounting and checkout.

c. SECTION III, CONTROLLER INSTRUCTION SET. Provides a listing and description of the command words which operate the controller and, in turn, are converted to commands for the disc drive.

d. SECTION IV, THEORY OF OPERATION. Provides an overall functional description and block diagram to the "board" level.

e. SECTION V, SERVICE. Provides preventive maintenance information, safety precautions, and flowcharts for troubleshooting analysis.

f. SECTION VI, REPLACEABLE PARTS. Provides ordering information for all field replaceable parts and assemblies on a "board-level" exchange basis.

1-3. GENERAL DESCRIPTION

1-4. The disc controller is a microprocessor-controlled device capable of connecting up to eight HP disc drives to an HP computer interface. The 13037D accommodates any combination of 7906D, 7920D and 7925D Disc Drives and one through eight computer interfaces.

1-5. The function of the controller is to translate high-level command words into commands which are intelligible to the disc drive. Along with the translation of commands, the controller transfers data bi-directionally between a disc drive and computer interface. In so doing, the controller takes steps to ensure data integrity. The computer interface is notified of any data transfer or control errors. A certain class of data error can be corrected by invoking software routines.

1-6. CONTROLLER ASSEMBLIES

1-7. Three printed-circuit assemblies (PCA's) and a chassis make up the controller; each PCA is an input/output (I/O) assembly that is plugged into the controller chassis. The PCA's are as follows:

- Microprocessor, part no. 13037-60001.
- Device Controller, part no. 13037-60028.
- Error Correct, part no. 13037-60024.

Additionally, a power regulator PCA is mounted in the controller chassis and supplies all necessary power to the above mentioned PCA's.

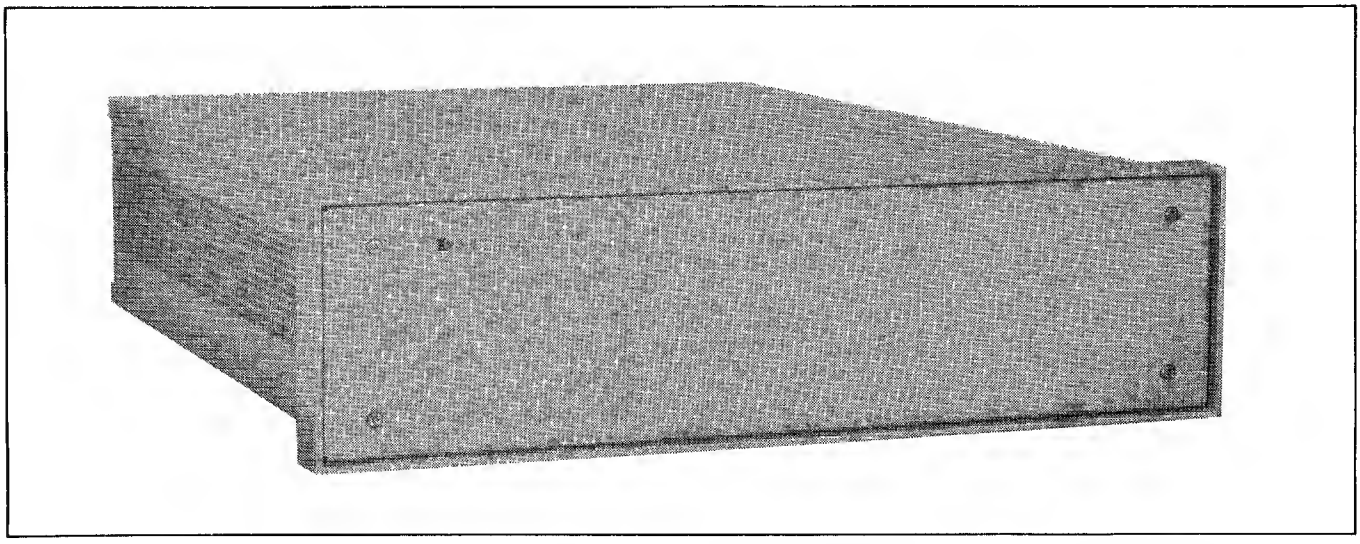


Figure 1-1. HP 13037D Disc Controller

1-8. AVAILABLE OPTIONS

1-9. The following options to the HP 13037D Disc Controller are available:

Opt 015 Operation on 240 Vac power
Opt 102 Adds HP 12745D HP-IB Adapter Kit

1-10. SERVICE DOCUMENTATION AVAILABLE

1-11. The following additional service documentation may be ordered from a Hewlett-Packard Sales and Support Office. Sales and Support Offices are listed at the back of this manual.

a. *HP 7906D Disc Drive Installation Manual,* part no. 07906-90912.

b. *HP 7906D Disc Drive Service Manual,* part no. 07906-90913.

c. *HP 7920D Disc Drive Installation Manual,* part no. 07920-90912.

d. *HP 7920D Disc Drive Service Manual,* part no. 07920-90913.

e. *HP 7925D Disc Drive Installation Manual,* part no. 07925-90912.

f. *HP 7925D Disc Drive Service Manual,* part no. 07925-90913.

g. *HP 12745D Disc Controller (13037) to HP-IB Adapter Kit Installation and Service Manual,* part no. 12745-90911.

INSTALLATION

SECTION II

2-1. INTRODUCTION

2-2. This section provides installation instructions for the controller. Included in these instructions are site preparation data, unpacking and inspection, installation procedures, claims procedures, and recommended packing and shipping methods.

2-3. SITE PREPARATION

2-4. Site preparation information for the controller includes environmental limitations, power requirements, and mounting considerations.

IMPORTANT NOTICE

The controller is a component part of a total system, and as such does not function independently. Therefore, when installing the controller into a complete system or peripheral product, assurances need to be made that the complete product complies with FCC Docket 20780 and VDE 0871 for Class A computing devices.

The controller is UL recognized and CSA certified as a component for use in complete data processing equipment. When installing the controller into a complete product, re-evaluation by an independent testing laboratory may be necessary to ensure that the combination of products used meets applicable safety standards.

2-5. ENVIRONMENTAL LIMITATIONS

2-6. Environmental limitations for operating and nonoperating conditions of the controller are specified in table 2-1. The environmental limitations imposed by other peripheral devices must be considered when these devices are located adjacent to the controller.

2-7. POWER REQUIREMENTS

2-8. The controller is shipped with the flexibility to operate from single-phase power mains of 100/120 volts at 2.8 amperes (typical) or 220/240 volts at 1.3 amperes (typical). (See figure 2-2.) The line voltage may vary -10 to +5 percent of the nominal value. The line frequency may vary from 47.5 to 66 Hz. Power consumption is 230 watts/2.3 amperes (typical) at 120V, 60 Hz.

Table 2-1. Controller Environmental Limitations

AMBIENT TEMPERATURE	
Operating:	0° to 55°C (32° to 131°F)
Nonoperating:	-40° to 75°C (-40° to 167°F)
ALTITUDE	
Operating:	4572 metres (15,000 feet) max
Nonoperating:	15300 metres (50,000 feet) max
RELATIVE HUMIDITY	
0 to 95% at 25° to 40°C (77° to 104°F) without condensation.	

2-9. Various safety codes require that instrument chassis, panels, and housings be grounded to protect operating and service personnel. A grounded three-conductor female power outlet must be made available to satisfy this requirement.

2-10. COOLING REQUIREMENTS

2-11. There are no external cooling requirements for the controller. With no restriction in airflow around the controller cabinet, internal fans provide adequate ventilation when operated within the environmental limitations specified in table 2-1.

2-12. MOUNTING CONSIDERATIONS

2-13. The controller is housed in a 133-millimetre (5-1/4-inch) by 425-millimetre (16-3/4-inch) by 584-millimetre (23-inch) chassis. A rack mount kit (part no. 13037-60012) is available to permit mounting the chassis in a standard 483-millimetre (19-inch) equipment rack. The weight of the controller is 15.9 kilograms (35 pounds) (with PCA's).

2-14. UNPACKING AND INSPECTION

2-15. When the controller shipment arrives, check to ensure receipt of the container as specified by the carrier's papers. Inspect the shipping container immediately upon receipt for evidence of mishandling during transit. If the container is damaged in any way, or if it is water-stained, request the carrier's agent be present when the container is opened.

2-16. Locate the packing list and open the shipping container. Compare this list against the purchase order to verify that the shipment is correct. Unpack the shipping container and inspect each item for ex-

ternal damage. Look for damage such as broken controls and connectors, dented corners, bent panels, scratches, and loose components. Check also the rigid foam-plastic cushioning (if used) for signs of deformation which could be indicative of rough handling during transit.

2-17. If the visual examination reveals any damage to the controller, follow the damage-claim procedure described in paragraph 2-42. Retain the shipping container and packing material for examination in the settlement of claims or for future reuse.

2-18. INSTALLATION PROCEDURE

2-19. The following paragraphs describe installations with the controller enclosed in a chassis. If the controller chassis is not used and the PCA's are installed separately, refer to the appropriate system document.

2-20. MANUAL UPDATING

2-21. Before installing the controller, perform any updating that may be required for the disc controller documentation. (A list of directly related hardware and software documentation is provided in paragraph 1-8 of this manual.) Updating instructions (if any) are provided with the appropriate document.

2-22. TOOLS AND TEST EQUIPMENT REQUIRED

2-23. TOOLS. No installation tools other than ordinary hand tools are required.

2-24. TEST EQUIPMENT. Test equipment required to verify adequacy of the ac mains voltage and proper adjustments of the controller power supply are listed in table 2-2.

Note: Even though the 30 MHz microprocessor PCA oscillator has an adjustable trim capacitor, no adjustment is required or should be made to the trimmer. Additionally, no adjustment should be made to the read circuitry trimmer on the device controller PCA.

2-25. AC POWER INSTALLATION AND VERIFICATION

2-26. AC POWER MAINS OUTLET AND EXTERNAL GROUND. The female power outlet to be used to supply ac power to the controller must be checked by a qualified electrician to ensure that it furnishes the proper voltage for which the controller is configured. The outlet and its associated wiring and fuses (or circuit breakers) must be capable of carrying the current specified in paragraph 2-7.

2-27. Figure 2-1 illustrates and provides the necessary details on the various ac power cord configurations available. Make sure that the local electrical code permits use of the type of power cord furnished with the controller.

2-28. Have a qualified electrician check the power outlet with an ac voltmeter to ensure that the required single-phase voltage is present. For proper operation of the controller, the mains voltage must be in the range specified in paragraph 2-7. Bear in mind that the electrical load imposed by the controller may reduce the line voltage below the nonload value.

2-29. If the line voltage is in the correct range, have the electrician check the power outlet to ensure that it is wired correctly with respect to ac high potential, ac neutral, and equipment ground. If the outlet is wired improperly, corrections must be made by a qualified electrician.

2-30. For safety reasons, it is mandatory that a connection be made between the controller "chassis ground" and cabinet "ground". Also required is a connection between cabinet "ground" and "earth". Refer to the appropriate site preparation manual for electrical connection requirements. For installation in a mobile environment (e.g., a ship, an aircraft or a train), the chassis ground wire in the controller ac power cord must be connected to the hull or metal frame of the vehicle.

Table 2-2. Installation Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED HP MODEL
Digital Voltmeter	At least four-digit readout. Minimum input impedance 10 megohms; fullscale ranges of 0.999 and 99.99 volts dc.	HP 3465B Digital Multimeter
AC Voltmeter	Battery-operated type capable of measuring ac power mains to ±2.0%. Voltage range must be from 88 to 132 volts ac or 176 to 264 volts ac.	HP 970A Probe Digital Multimeter

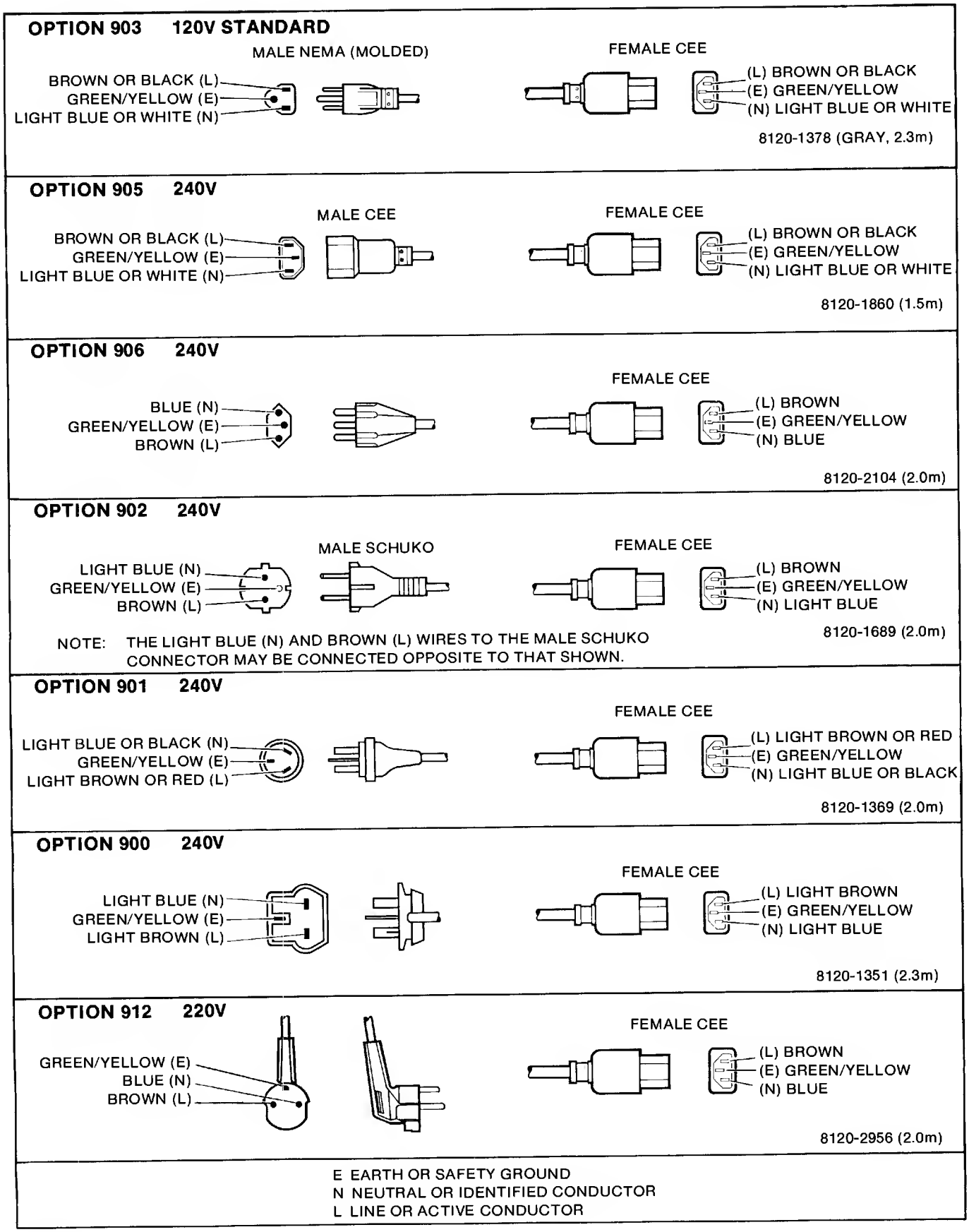


Figure 2-1. AC Power Cord Sets

IMPORTANT NOTICE

The controller is wired at the factory for either 120 Vac or 240 Vac (Option 015) input voltage. A reversible label on the rear panel (see figure 2-5) denotes the wiring configuration. The 120 Vac configuration can be changed to 100 Vac operation and the 240 Vac configuration can be changed to 220 Vac by changing the strapping on the transformer barrier block. *No other wiring configurations are permissible.*

WARNING

To avoid personal injury, disconnect the power cord from the power source before changing a strapping configuration.

2-31. If the primary power source is other than that noted on the wiring configuration label (see figure 2-5), disconnect the power cord and change the strapping on the transformer barrier block according to figure 2-2. Make sure that the wiring configuration label matches the strapping configuration. Refer to the replaceable parts list for label part numbers.

2-32. FUSE RATING CHECK. The controller is equipped with one primary power fuse (F1) and one secondary fuse (F2).

WARNING

Observe the warning label affixed to the rear panel when replacing the primary power fuse.

WARNING

To install or remove a fuse, first disconnect the power cord from the device. Then, using a small screwdriver, turn the fuseholder cap counterclockwise until the cap releases. Install the proper fuse in the cap — either end of the fuse can be installed in the cap. Next, install the fuse and fuseholder cap in the fuseholder by pressing the cap inward and then turning it clockwise until it locks in place.

2-33. The primary power fuse is a time delay (slow-blow) fuse and is located on the rear panel. Check that the rating of the primary power fuse conforms to the rating specified in table 2-3. The secondary fuse is located on the power supply PCA. This fuse protects the +5 Vdc power supply. The required rating is 25A, 32V, standard (part no. 2110-0250).

Table 2-3. Primary Power Fuse Rating

SOURCE	RATING	HP PART NO.
100 Vac	4A, 250V, SB	2110-0365
120 Vac	4A, 250V, SB	2110-0365
220 Vac	2A, 250V, SB	2110-0303
240 Vac	2A, 250V, SB	2110-0303

2-34. MOUNTING INSTRUCTIONS

2-35. For most installations, the controller will be rack mounted in an equipment cabinet. The rack

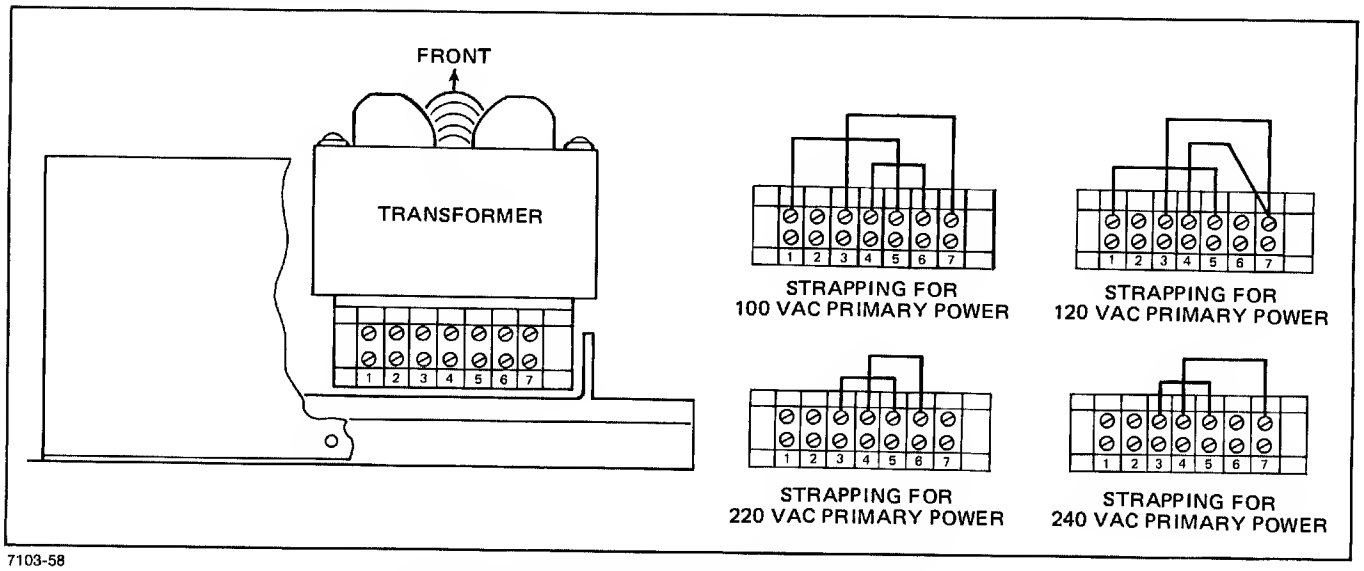


Figure 2-2. Transformer Strapping Configurations

mounting kit, model no. 13037R, is available for mounting the controller in an equipment cabinet. Mount the rails to the inside of the equipment cabinet according to the instructions furnished with the kit. Then install the controller to the equipment cabinet with four no. 10-32 rack-mounting screws. Two screws are used on each side of the mounting flange.

2-36. POWER SUPPLY CHECK

2-37. Check the power supply voltages. Table 2-4 lists the power supply voltage ranges. The +5 Vdc is the only portion of the power supply that can be adjusted. Figures 2-3 and 5-1 show the test point and adjustment locations.

2-38. Plug the controller power cord into the power outlet and proceed as follows:

a. Remove the top cover.

WARNING

Hazardous voltages are exposed when the top cover is removed.

b. On rear panel, set POWER switch to 1 (on).

c. Connect digital voltmeter between the required test point and COM to check voltages.

d. If the +5V power supply is not within range, adjust +5V potentiometer (see figure 2-3) to obtain voltage level listed in table 2-4.

e. Set POWER switch to 0 (off).

f. Disconnect voltmeter and replace top cover on controller.

2-39. CONTROLLER PCA CONFIGURATION

2-40. The PCA configuration is shown in figure 2-4. The microprocessor and device controller PCA's can be installed in either of the two lower card slots, but must be connected by jumper cable 13037-60021 at the center connector.

2-41. CONTROLLER INTERCONNECTIONS.

Proceed with the controller interconnections as follows:

a. Remove the top cover and front panel from the controller.

b. Remove the cable bracket assembly from the rear of the controller and separate the two brackets (see figure 2-5, view A).

c. Locate and completely remove the clear piece of shrink tubing from the HP 13013D Multi-Unit Cable to expose the small area of shield braid. Use extreme care to prevent damaging the cable.

d. Locate the package of hardware attached to the multi-unit cable. The package includes the following:

(1) Two 6-32 nuts, part no. 2420-0003.
(2) Two 6-32 screws, part no. 2360-0183.
(3) One clamp, part no. 5021-1604.
(4) One spacer, part no. 5001-3320.
(5) One clamp, part no. 5021-1603.

e. Mount the hardware on the multi-unit cable oriented as shown in figure 2-5, view A. Make sure that the 5021-1604 clamp makes firm contact with the exposed shield braid.

f. Locate and completely remove the clear piece of shrink tubing from the interface or multi-CPU (13175D/13178D Interface Kits) to expose the small area of shield braid. Use extreme care to prevent damaging the cable.

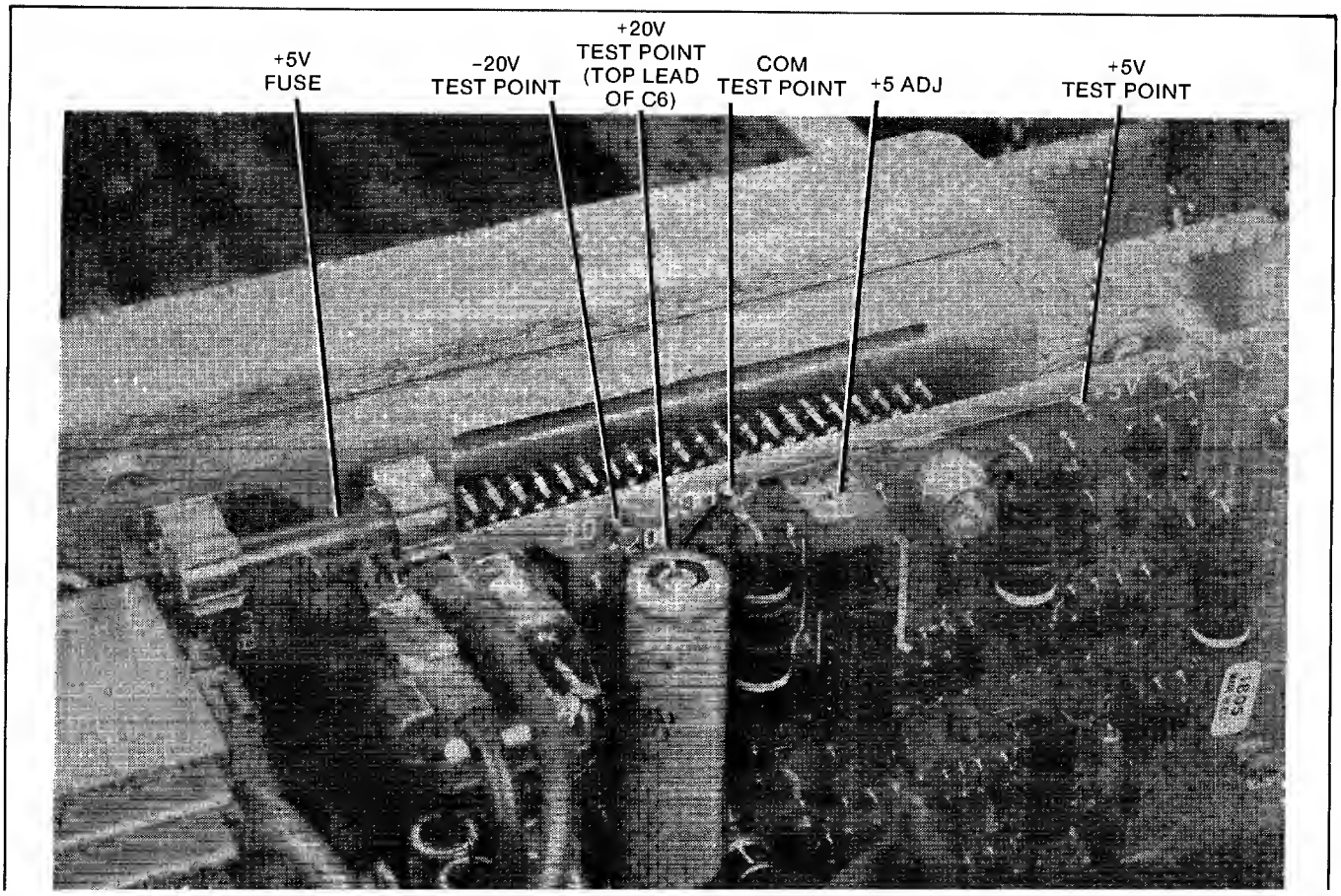
g. Locate the package of hardware attached to the cable. Refer to step d for a list of the contents.

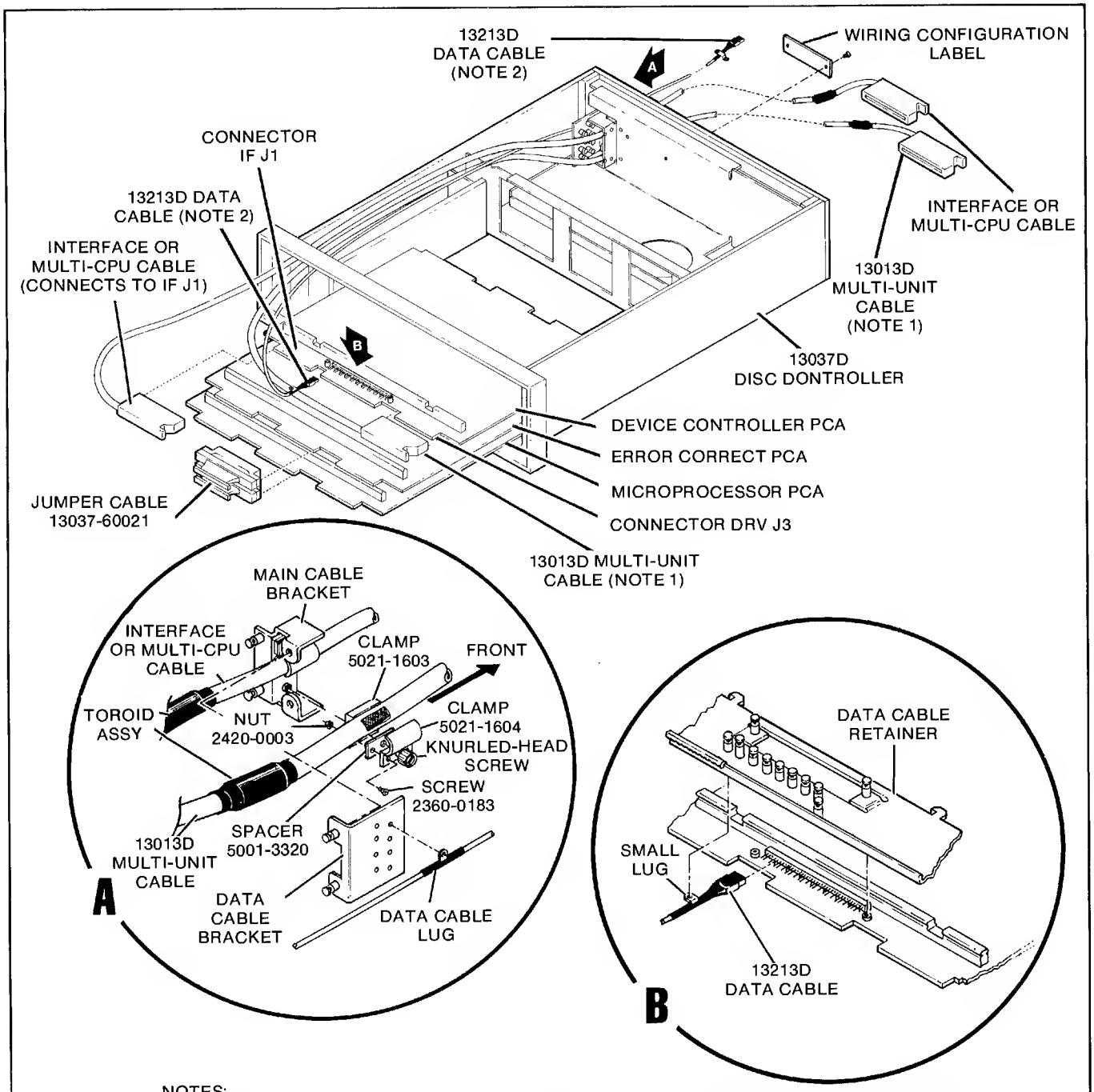
h. Mount the hardware on the cable oriented as shown in figure 2-5, view A. Make sure that the 5021-1604 clamp makes firm contact with the exposed shield braid.

i. Locate and completely remove the clear piece of shrink tubing covering the lug of each HP 13213D

Table 2-4. Power Supply Voltages

SUPPLY	SPECIFICATIONS
+5V Regulated	Voltage: +4.95 to +5.05 Vdc (adjustable) Ripple and Noise: < 1 mV rms
-5V Regulated	Voltage: -4.75 to -5.25 Vdc (nonadjustable) Ripple and Noise: < 5 mV rms
+20V Unregulated	Voltage: +18 Vdc nominal (nonadjustable) Ripple: ≤ 3.1V p-p @ maximum load
-20V Unregulated	Voltage: -18 Vdc nominal (nonadjustable) Ripple: ≤ 3.1V p-p @ maximum load


+5V
FUSE
-20V
TEST POINT
+20V
TEST POINT
(TOP LEAD
OF C6)
COM
TEST POINT
+5 ADJ
+5V
TEST POINT



NOTES:

1. THE HP 13013D MULTI-UNIT CABLE IS AVAILABLE IN FOUR LENGTHS AS FOLLOWS. MAXIMUM CUMULATIVE CABLE LENGTH, CONTROLLER TO LAST DISC DRIVE, IS 25.55 M (74 FT).

CABLE	PART NO.	LENGTH
13013D-001	13013-60024	1.83 M (6 FT)
13013D-003	13013-60025	2.44 M (8 FT)
13013D	13013-60027	3.66 M (12 FT)
13013D-002	13013-60028	5.49 M (18 FT)

2. THE HP 13213D DATA CABLE IS AVAILABLE IN FIVE LENGTHS AS FOLLOWS:

CABLE	PART NO.	LENGTH
13213D-004	13213-60011	1.83 M (6 FT)
13213D	13213-60012	3.05 M (10 FT)
13213D-001	13213-60013	7.62 M (25 FT)
13213D-002	13213-60014	15.24 M (50 FT)
13213D-003	13213-60015	22.86 M (75 FT)

REF 7301-76D

Figure 2-5. Controller Interconnection Diagram

Data Cable to be installed. Use extreme care to prevent damaging the black shrink tubing or the cable.

j. Secure the two cables prepared in steps e and h to the main cable bracket, oriented as shown in figure 2-5, view A, using the attached knurled-head screws.

k. Secure all data cables prepared in step i to the data cable bracket with the attached spring-loaded captive screws (see figure 2-5, view A). Any of the eight positions may be used.

l. Attach the data cable bracket to the main cable bracket with the two attached captive screws.

m. Pass the cables through the opening at the rear of the controller and secure the cable bracket assembly to the controller with the two attached captive screws. Be sure that none of the toroid assemblies on the cables are within the controller.

n. Position the cables in the channel provided and lying to the right of the fan.

o. Connect each data cable to the device controller PCA at connectors J4 through J11.

Note: Any data cable may be connected to any of the connectors on the PCA.

p. Secure each data cable to the data cable retainer assembly on the PCA with the attached spring-loaded captive screws (see figure 2-5, view B).

q. On the controller, ensure that the jumper cable, part no. 13037-60021, is connected between connector J2 on the error correct PCA and connector J2 on the microprocessor PCA.

r. Connect the interface cable to the device controller PCA at connector IF J1.

s. Connect the multi-unit cable to the device controller PCA at connector DRV J3.

t. Replace the controller top cover and front panel.

u. Replace and secure the controller.

v. Connect the ac power cord from the controller to an appropriate ac power source.

w. When one or more disc drives are installed, the logical unit address of each must be specified to the controller. The position of the UNIT SELECT switch determines the logical unit address of the disc drive. Ensure that no two disc drives have the same logical unit address.

2-42. CLAIMS PROCEDURE

2-43. If the shipment is incomplete or if the equipment is damaged or fails to meet specifications, notify the nearest Hewlett-Packard Sales and Support Office. If damage occurred in transit, notify the carrier as well. Hewlett-Packard will arrange for replacement or repair without waiting for settlement of claims against the carrier. In the event of damage in transit, retain the shipping container(s) and packaging material for inspection.

2-44. REPACKAGING FOR SHIPMENT

2-45. The following paragraphs provide instructions for repackaging the controller for shipment. Included are instructions for shipping the controller using the original packaging or new packaging.

2-46. SHIPMENT USING ORIGINAL PACKAGING

2-47. The same containers and materials used in factory packaging can be used for reshipment of the controller. Alternatively, the correct containers and packing materials may be obtained from Hewlett-Packard Sales and Support Offices. Use the following instructions as a guide when packaging the controller with the original factory packaging materials:

a. If the controller is being sent to the factory for servicing, attach a tag specifying the return address, type of service or repair required, model number, and full serial number.

b. Seal the shipping container securely and mark it "FRAGILE" to ensure careful handling.

c. In any subsequent correspondence with the factory, refer to the controller by model number and full serial number.

2-48. SHIPMENT USING NEW PACKAGING

2-49. The following instructions should be used as a guide when packaging the controller with commercially available materials:

a. Wrap the controller in heavy paper or sheet plastic. If the controller is being sent to the factory for servicing, attach a tag specifying the return address, type of servicing or repair required, model number, and full serial number.

b. Use a strong shipping container. A double-wall carton constructed of 158.9-kilogram (350-pound) test material is adequate.

c. Use sufficient shock-absorbing material on all sides of the controller to provide a firm cushion

and to prevent movement inside the container. Use particular care to protect the controller corners and chassis.

d. Seal the shipping container securely and mark it "FRAGILE" to ensure careful handling.

e. In any subsequent correspondence with the factory, refer to the controller by model number and full serial number.

CONTROLLER INSTRUCTION SET

SECTION III

3-1. INTRODUCTION

3-2. To give the reader a better understanding of the relationship between the controller and disc drive, some disc drive characteristics and the controller instruction set are discussed in this section. For complete disc drive characteristics, refer to the appropriate disc drive documentation.

3-3. TRACK RECORDING FORMAT

3-4. Each disc track is divided into equal sectors which are derived by counting markers on a servo track. Each sector is identified by a sector number and address. The location of sector 0 is found by an index mark (see figure 3-1). Disc drive circuitry identifies the sectors. In the circuitry, a counter is incremented by one when each sector is sensed and reset to zero when the index marker is sensed.

3-5. When the controller issues a SEEK address to the drive, that address includes a sector number. After issuance the controller disconnects from the disc drive and the computer which issued the command. The controller can then service other computers or other discs if available while waiting for the seek to complete. The disc drive can notify the controller that the seek is complete when the heads have reached the proper cylinder or when the heads have reached the proper cylinder and sector address at a certain number of sectors before the destination address toward which the disc is rotating. This latter mode is called "rotational position sensing" or RPS.

3-6. SECTOR RECORDING FORMAT

3-7. The smallest addressable data storage area in the disc drive is a sector. Accessing a sector is accomplished by specifying the address of the cylinder, head, and sector. The sector recording format is shown in figure 3-2. Each sector contains a sector address field, a data field, and data checking and error correction fields. The sector address field contains the cylinder, head, and sector addresses of the sector, as well as indicators for spare, defective, and protected tracks. The data field stores 128 words of data. Each data word is defined as 16 bits. Only the data field is transferred to and from the computer in most data operations. The preamble and postamble are normally generated and checked in the controller. All fields except the sync are error checked by the controller.

3-8. COMMAND OPERATIONS

3-9. To initiate an operation, the controller accepts a 16-bit command word from the CPU interface, then decodes, and executes the operation specified. The command may pertain to the controller only, a selected disc drive only, or both. Some commands require additional information from the interface for proper execution. Each command is discussed separately in the following paragraphs.

3-10. The command word format relating to a specific command is shown at the beginning of each paragraph. Bits 8 through 12 of the command are used for the opcode, that is, the octal representation that identifies each command. The U referred to in the

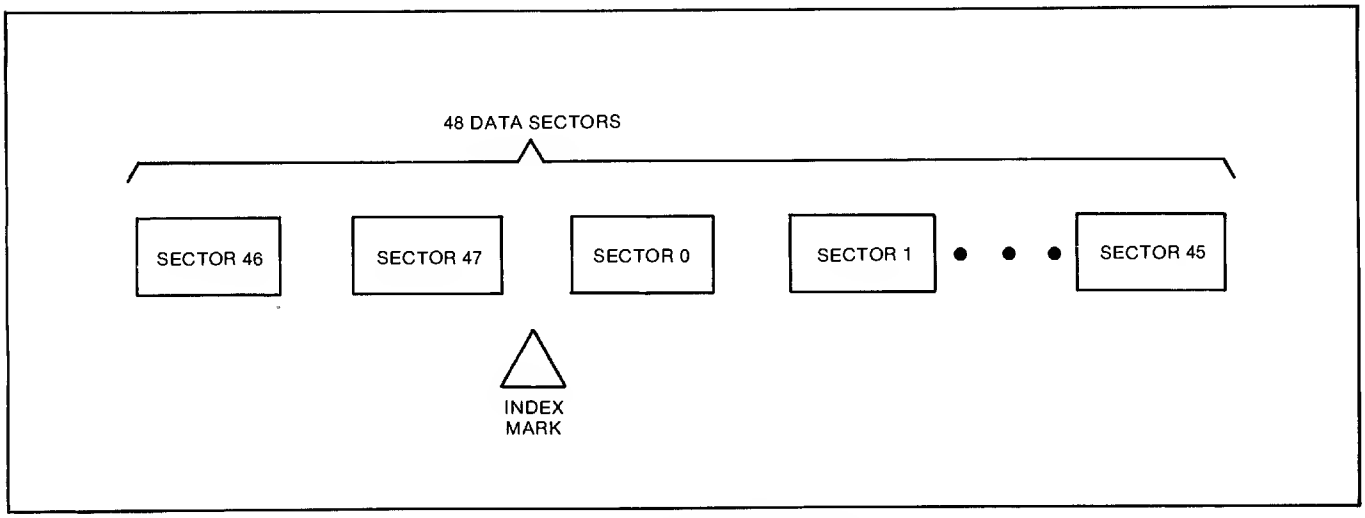
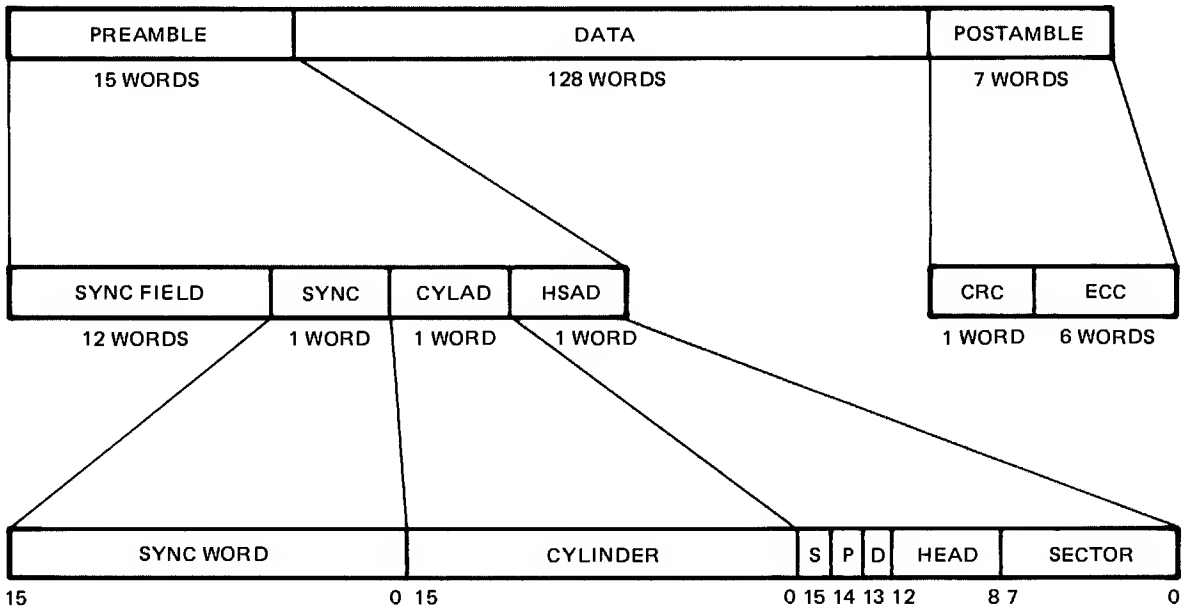


Figure 3-1. Track Recording Format

command format is the disc drive unit number. (The cross-hatched bits indicated in some of the command words are not processed by the controller.) Table 3-1 is a listing of command codes and commands. The commands are listed functionally as control, sense, read, and write groups. They are also discussed in the following paragraphs according to their functional group. The timeout function referred to in the discussion is approximately 1.8 seconds.

3-11. Each disc drive has a "hold" bit associated with it to prevent two different CPU interfaces from accessing the same disc drive at the same time. Each command to the controller which references a disc drive (except Request Status and Request Sector Address) includes a one-bit hold field which is retained by the controller. While a hold bit is set for a particular disc drive, no other CPU interface may access it with a command that could modify the disc drive status. A command which requires such access to a "held" disc drive is buffered on the interface until the drive becomes available. Whenever a drive is thus found to be unavailable, the controller resumes polling.

3-12. Sparing, as referred to in the discussion, is the automatic "seek to read from" or "seek to write to" tracks which replaced defective tracks, using cross reference addresses in the CYLAD and HSAD fields of the preamble. Such a seek can be enabled or disabled with the SET FILE MASK command (see paragraph 3-27). When sparing is required and enabled, it occurs at the beginning of all data transfer commands which verify a sector before starting the transfer and whenever a new track is accessed during a multiple-sector data transfer. (Exceptions are noted in the discussion of the individual commands.)



PREAMBLE – 15 WORDS FOR SYNCHRONIZATION AND ADDRESSING
DATA – 128 WORDS OF DATA
POSTAMBLE – DATA CHECKING AND ERROR CORRECTION INFORMATION
SYNC FIELD – 12 WORDS (192 BITS) OF Ø'S
SYNC – SYNC WORD – 100376_8 IF ECC FIELD IS VALID
– 100377_8 OTHERWISE
CYLAD – CYLINDER – CYLINDER ADDRESS
HSAD – HEAD ADDRESS (LOGICAL)
SECTOR ADDRESS (LOGICAL)
S – IF "1", SPARE TRACK IN ACTIVE USE
P – IF "1", PROTECTED TRACK
D – IF "1", DEFECTIVE TRACK
CRC – CYCLIC REDUNDANCY CHECK – 1 WORD OF CHECK INFORMATION
ECC – ERROR CORRECTION CODE – 6 WORDS OF CHECK AND CORRECTION INFORMATION

7300-37B

Figure 3-2. Sector Recording Format

Table 3-1. Command Codes

OCTAL CODE (BITS 8-12)	COMMANDS BY GROUP			
	CONTROL	SENSE	READ	WRITE
00			Cold Load Read	
01	Recalibrate			
02	Seek			
03		Request Status		
04		Request Sector Address		
05			Read	
06			Read Full Sector	
07			Verify	
10				Write
11				Write Full Sector
12	Clear			
13				Initialize
14	Address Record			
15		Request Syndrome		
16			Read with Offset	
17	Set File Mask			
22			Read without Verify	
23		Load TIO Register		
24		Request Disc Address		
25	End			
26	Wakeup			

3-13. The mnemonics used in the command descriptions are the following:

a. Controller to CPU Interface:

CLEAR — Hard clear on controller logic
ENID — Enable Interface Drivers
ENIR — Enable Interface Receivers
IBUS 0-15 — Data Bus
IFN 0-3 — Function Bus
IFCLK — Interface Clock (Validates Data Bus)
IFVLD — Interface Function Valid

b. Flags from Interface:

CMRDY — Command Ready
DTRDY — Data Ready
EOD — End of Data
INTOK — Interrupt O.K.
OVRUN — Overrun
XFRNG — Transfer No Good

c. Function Bus Commands:

BUSY — Set or Clear Interface Busy Bit
DSCIF — Disconnect Interface
DVEND — Device End
IFIN — Data In, Controller to Interface
IFGTC — Get Command from Interface
IFOUT — Data Out, Interface to Controller
IFPRF — Pre-fetch Command from Interface
RQSRV — Request Service
SELIF — Select Interface
SRTRY — Set Retry Counter
STDFL — Set Data Flag
STINT — Set Interrupt
WRTIO — Write Interface Status Register

The hardware implementation of these mnemonics is discussed in section IV.

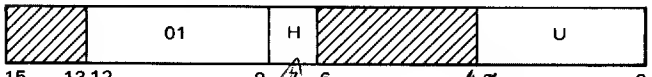
3-14. CONTROL COMMANDS

3-15. There are seven control commands issued by the interface for the controller to start disc drive operations which do not involve the transfer of data between the controller and computer. These include the following: recalibrate, seek, clear, address record, set file mask, end, and wakeup. For most of these commands, the entire operation to be started is specified by the control command. When a command is accepted by the controller and a disc drive is available, the busy bit of the calling interface is set. At command completion, the busy bit is cleared. Note that

RQSRV is issued after every transfer of control information (other than the command word) and after every data transfer; this happens for all commands of all of the following functional groups.

3-16. RECALIBRATE

CONTROL COMMAND 1



H = Hold bit U = Unit number

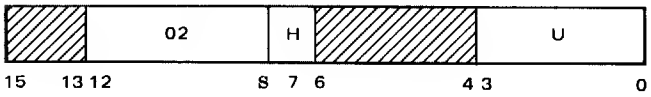
7103-16

3-17. The RECALIBRATE command word contains an opcode, a hold bit, and a unit number. If the addressed unit is available and ready, the controller sends the RECALIBRATE command to the drive and then returns to the poll loop. (Refer to Controller Polling in section IV.) The disc drive positions its head over cylinder 0 and clears its current cylinder-address register. When the drive completes this recalibration function the drive's attention bit is set (see table 4-3).

3-18. If Interrput O.K. (INTOK) is true, the controller transmits Set Interrupt (STINT) to the interface and clears the drive's attention bit. The computer must always wait for STINT before issuing the next command. In the case where the unit is not ready when it is called, the controller does not wait for RECALIBRATE but immediately returns STINT to the interface and waits for another command to be issued or a timeout.

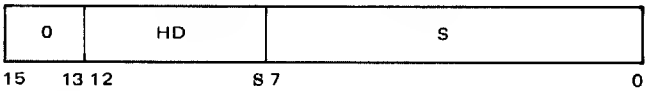
3-19. SEEK

CONTROL COMMAND 2



CYLINDER ADDRESS

HEAD-SECTOR ADDRESS



H = Hold bit HD = Head address
U = Unit number S = Sector address

7103-17

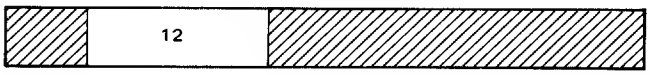
3-20. The SEEK command causes drive positioner motion. It is initiated by issuing the command word followed by two address words in the order shown. The controller requests each of the address words by transmitting STDFL (Set Data Flag) to the interface. The first address word contains the cylinder address and the second contains the head and sector address. The addresses are transmitted to the disc drive and the controller begins polling while waiting for seek completion. When seek has completed, the drive sets an attention bit to notify the controller. When the poll reaches a disc drive which has an attention bit set and the corresponding interface Interrupt O.K. (INTOK) flag is true, the controller interrupts the interface and clears the disc drive's attention bit. An interface can avoid the attention interrupt by sending a command (e.g., READ) while the drive is seeking. The controller will buffer the READ command until the SEEK has completed. This approach is not recommended in a multiple-interface subsystem because the controller cannot use the seek time to service commands from other interfaces.

3-21. The cylinder, head, and sector addresses of the current seek are retained in the controller memory for future operations but they will be overwritten by any subsequent ADDRESS RECORD or SEEK command. Since the controller polls the other interfaces before reporting a seek completion, the program should issue an ADDRESS RECORD command immediately preceding a data transfer operation if another interface is active in the disc subsystem.

3-22. If the drive unit is available but will not respond, the controller sends STINT (Set Interrupt) to the interface after accepting the address words. The interface busy bit will be set. The controller then waits for a new command to be issued from the interface or for a timeout.

3-23. CLEAR

CONTROL COMMAND 3

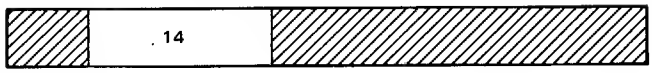


7103-18

3-24. Upon receipt of a CLEAR command from the interface, the controller will issue a CLEAR to clear all drives, clear status, clear any clock offset, clear the interface busy bit, transmit STDFL (Set Data Flag) to the interface, and wait for a new command or for a timeout. A unit number is not required. A controller "power on", or hard clear (preset) from an interface, also causes the controller to clear all drives. Be cautious in using this command because if another interface is active in the disc subsystem, it will clear any drive held by that interface.

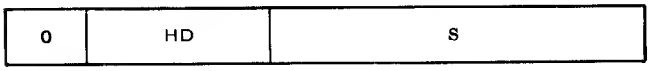
3-25. ADDRESS RECORD

CONTROL COMMAND 4



CYLINDER ADDRESS

HEAD-SECTOR ADDRESS



HD = Head address S = Sector address

7103-19

3-26. The ADDRESS RECORD command is used to set a logical address in the controller without transmitting it to the disc drive. The issuance of the command word is followed by two address words in the order shown. The first contains the cylinder address and the second contains the head and sector address. The controller requests each of these words by transmitting STDFL to the CPU interface. Upon receipt, the controller transmits Request Service (RQSRV) to the interface and waits until either a command is received or a timeout occurs. Polling is suspended on completion of this command. If used in a multiple computer environment, an ADDRESS RECORD should follow each SEEK or RECALIBRATE command, or should precede a data transfer operation if the SEEK or RECALIBRATE is not used.

3-27. SET FILE MASK

CONTROL COMMAND 5

7103-20A

The "set file mask" bit functions are as follows:

Bit 0 Allows automatic seek as per bit 3 if set (logical 1).

Bit 1 If set (cylinder mode), a logical cylinder consists of all available surfaces at the current track address and the end-of-logical-cylinder occurs when last sector of surface has been transferred. If clear (surface mode), a logical cylinder consists of the sectors at the current track and head address and the end-of-logical-cylinder occurs when the last sector of any surface has been transferred.

Bit 2 Allows automatic seek to spare track (sparing enabled).

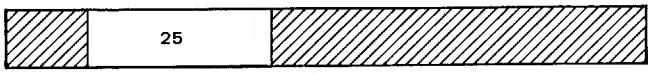
Bit 3 If set, decremental seek at end-of-logical-cylinder is selected. If not set, incremental seek at end-of-logical-cylinder is selected. If bit 0 = 0, this bit is ignored.

Bit 4-7 Number of retries allowed (3000 systems only).

3-28. The SET FILE MASK command sets the mode of operation for the controller. The controller transfers bits 0-3 into its "mask" register which is used to control the action taken while transferring data. The entire word is transmitted to the interface via a Set Retry Counter (SRTRY) order. For computers with a data channel separate from the CPU, the retry counter allows the channel program to retry a data transfer in case of an error. The programmer sets the counter with bits 7 through 4 of this command. After the specified number of retries, the interface (not the controller) interrupts the CPU. After sending SRTRY, the controller transmits Set Data Flag (STDFL) to the interface. Polling is suspended on completion. The controller takes no further action until a command is received or a timeout occurs. At power up or timeout, the mask is set to no-automatic-seek, surface mode, and no sparing.

3-29. END

CONTROL COMMAND 6

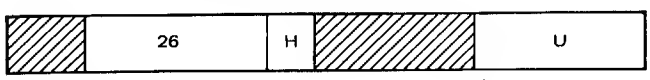


7103-21

3-30. The END command is used to avoid a timeout if no other command is expected to be output from an interface and the controller is waiting for a command from that interface. When the controller accepts this command from an interface, no action is taken except to resume polling. This command should follow any string of commands when they have been completed.

3-31. WAKEUP

CONTROL COMMAND 7



U = Unit number

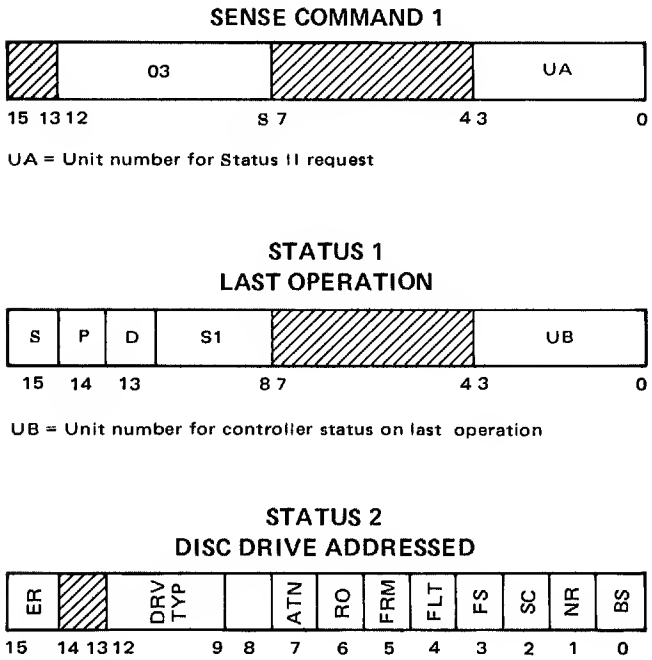
7103-22A

3-32. The WAKEUP command checks if the specified unit is available (connected to current interface or hold bit clear). If not, the command is left pending on the interface and the controller resumes interface polling. If the unit is available, the status register is set to indicate "unit available" and STDFL is transmitted to the interface. The controller then waits until a command is received or until timeout occurs. This command may be omitted in single-interface subsystems. It should precede all command sequences in multiple-interface subsystems.

3-33. SENSE COMMANDS

3-34. There are five sense commands to determine the status of the disc drive and controller as well as to identify the specific nature of any errors or unusual conditions that have occurred. The "request status" command gets information on the last operation and status of the addressed disc drive. The "request sector address" command obtains the current sector address from the disc drive, and the "request syndrome" command is used for detected errors which may be correctable. The "load TIO register" command is a diagnostic tool, and the "request disc address" command returns the address words currently stored in the controller. This last command is generally used after an error interrupt so that the operating system can find where it occurred. Returned information is accompanied by a STDFL flag, telling the interface that data has been returned.

3-35. REQUEST STATUS



UA Unit number to which Status-2 (drive status) request will be issued.

UB Unit number to which controller status on last operation applies. If S1 is 37 (drive attention), U is the number of the interrupting drive. If no unit number is appropriate (S1 = 01 or 12), UB will be zero.

S1 Encoded controller termination status (octal).

S Spare Track

P Protected Track

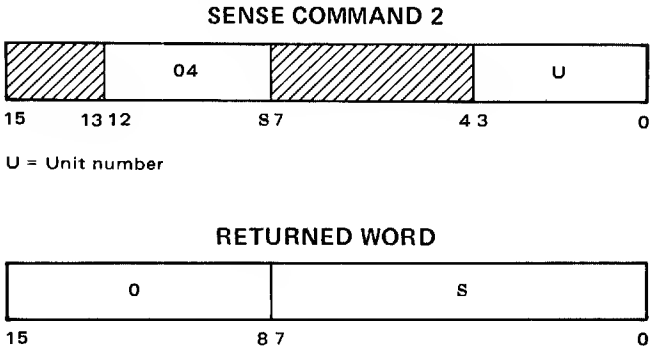
D Defective Track

The various encoded termination status values in the S1 field are explained in table 3-2.

3-36. After receipt of the REQUEST STATUS command, the controller returns two status words to the interface. The first (Status 1) contains information relating to the last operation performed, and the second (Status 2) contains information pertaining to the disc drive addressed in the command word. The First Status Bit in Status 2 is cleared by this command after it is reported. The controller then waits for a command from the same interface or for a timeout to occur.

Note: The Status 1 word is also transmitted to the interface at the completion of all commands or at an error interrupt. The WRTIO function bus command is used.

3-37. REQUEST SECTOR ADDRESS



3-38. After receipt of the REQUEST SECTOR ADDRESS command, the controller returns the logical address of the sector currently passing under the heads of the specified unit. The existing hold bit is not checked or altered. Polling is suspended on completion.

Table 3-2. Request Status Fields

STATUS 1: CONTROLLER STATUS LAST OPERATION

00 NORMAL COMPLETION. Transmitted in one of two situations:

a. When command has been fully executed without error.

b. At completion of a REQUEST STATUS command when it is the first command issued after interface is connected to controller during a polling sequence. In this case, the U field is zero.

01 ILLEGAL OPCODE. A command word has been received by the controller of which bits 12-8 contain a command code which is not one of controller's command set.

02 UNIT AVAILABLE. Controller transmits this status after interface has put out a WAKEUP command for a specific drive and that drive has become available.

07 CYLINDER COMPARE ERROR. During verification of address of sector preceding the address of first sector to be read from or written to, the contents of cylinder address field of that sector do not match contents of controller's cylinder address register. When this status is received, the system should issue a RECALIBRATE command and then retry data transfer sequence. This status is transmitted only after the sequence of events listed below.

a. Addresses do not compare as described above.

b. Controller generates a seek-to-address from its cylinder address register and head-sector address register.

c. Controller again attempts to verify a sector.

d. Addresses still do not compare.

e. The S bit is not set at new track address.

10 UNCORRECTABLE DATA ERROR. This status is generated by the error correction circuits and is transmitted in one of three cases:

a. Immediately following a data transfer (or VERIFY) command if error is uncorrectable.

b. In response to a REQUEST SYNDROME command whenever a Possibly Correctable Data Error has proved uncorrectable.

c. During sector address verification preceding the address of first sector to be read from or written on, the controller cannot read (verify) and of 16 consecutive sectors without error.

11 HEAD-SECTOR COMPARE ERROR. Similar to Cylinder Compare Error, including controller's recovery attempt sequence described for that status, except that in this case the head and/or sector address fields of the disc sector do not compare with corresponding fields in the controller's head-sector address register. The system need not issue a RECALIBRATE command when this status is received.

12 I/O PROGRAM ERROR. The interface of systems containing a programmable data channel separate from the CPU may detect abnormal channel operations and notify the controller. At that time, controller will interrupt the CPU with this status. An example of such an error might be an inconsistent direction of data transfer (a READ command has been transmitted to controller, but channel has been programmed to write).

14 END OF CYLINDER. A multiple-sector data transfer must continue beyond end-of-logical-cylinder, but file mask will not allow controller to automatically seek to next logical cylinder and continue.

16 OVERRUN. Detected by interface (read) or controller (write) whenever the instantaneous data rate of controller exceeds that of the CPU-interface combination. The overrun is reported at end-of-sector in which it occurred. The contents of that sector, either on disc (write) or in I/O buffer (read), should be considered invalid.

Note: The controller always transfers complete sectors. If CPU or data channel wishes to transfer less than a complete sector, it must notify interface (or controller) when transfer is complete so that subsequent controller requests for data transfer do not cause an overrun error.

Table 3-2. Request Status Fields (continued)

17 POSSIBLY CORRECTABLE DATA ERROR. This status is generated by the error correction circuits and is transmitted in one of two cases as follows:

a. Immediately following a data transfer (or VERIFY) command if error is possibly correctable.

b. In response to a REQUEST SYNDROME command if error is in fact correctable. In this case, proceed as described in REQUEST SYNDROME command.

20 ILLEGAL ACCESS TO SPARE TRACK. The same conditions and sequence of events described for a Cylinder Compare error or Head-Sector Compare Error have occurred, except that S bit is set at a new track address. This error usually results from trying to directly access (via a SEEK command) a spare track in active use. The addresses will not compare because of the way in which spare tracks are set up and this status merely differentiates between this situation and other address errors.

21 DEFECTIVE TRACK. Detected during verification of track status of the sector preceding the address of the first sector to be read from or written on. Defective track status is issued when the D bit is found to be set but File Mask will not allow automatic seeking to a spare track. This status is also issued if the D bit is set but the spare track address is the same as the defective track address.

← check seek time adjustment (A3 card)

22 ACCESS NOT READY DURING DATA OPERATION. While in the process of transferring data to or from the disc, the track center detector in the drive detected head motion. The transfer should be retried.

23 STATUS 2 ERROR. The controller is unable to complete a command due to some condition in the disc drive. The Status 2 word may be examined for reason. Examples of Status 2 Errors are:

a. An Initialize command, but FORMAT switch is off or PROTECT (READ ONLY) switch is on.

b. A SEEK command is issued to a drive which is Not Ready (heads unloaded).

26 ATTEMPT TO WRITE ON PROTECTED TRACK. Status detected during verification of track status of the sector preceding the first sector to be written on using a Write command. This status information is issued when the P bit is found to be set and the FORMAT switch is off.

27 UNIT UNAVAILABLE. This status is returned whenever the U field of the command word is greater than 7 (octal).

Note: The interface busy bit is false whenever this status is returned.

37 DRIVE ATTENTION. Controller generates an interrupt (issues STINT) to the interface which last accessed the drive which is requesting attention (or to interface 0 if this is the first attention after power-on or hard clear) whenever all of the following occur:

a. Drive is requesting attention.

b. Interface does not have a subsequent command pending in its command buffer excepting WAKEUP, which is ignored here.

c. Interface flag INTOK (Interrupt O.K.) is set, thereby allowing attention interrupts.

Briefly, conditions causing a drive to request attention are the following:

a. Seek completion.

b. Drive becomes ready (heads load).

c. Drive becomes not ready (heads unload).

d. Seek check, illegal cylinder address.

e. Drive Fault.

Refer to the appropriate Disc Drive User's Manual for a more complete description of these conditions.

Table 3-2. Request Status Fields (continued)

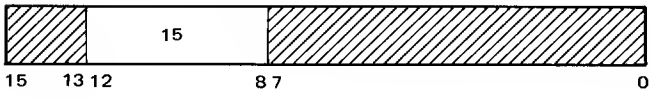
STATUS 2: STATUS OF DISC DRIVE ADDRESSED BY STATUS COMMAND

S2 Unit status

Bit	
0*	Drive busy (BS)
1*	Drive not ready (heads not loaded) (NR)
2*	Seek check (SC)
3	First status (FS)
4*	Fault (FLT)
5	Format (FRM)
6	Upper/Lower Protect or Read Only (RO)
7	Attention (ATN)
8	(Reserved)
9-12	Encoded drive type (used by controller to determine last available head and sector) (DRV TYP)
15	Status 2 error (true if any bit marked * is true) (ER)

3-39. REQUEST SYNDROME

SENSE COMMAND 3



7103-25

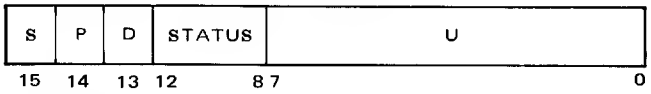
3-40. The REQUEST SYNDROME command is used when errors have been detected by the controller after transferring data from the disc drive to the computer. The command may be issued after a READ, COLD LOAD READ, READ WITH OFFSET, VERIFY or READ WITHOUT VERIFY command which terminates with a Status 1 word indicating "Possibly Correctable". The software correction routine should not try to correct the preamble or postamble since these areas have not been transmitted to the data buffer in the computer.† See figure 3-2 for the sector recording format and related nomenclature pertaining to this discussion.

3-41. The REQUEST SYNDROME command should only be issued if the Status 1 field immediately following a data transfer (or VERIFY command) contains "Possibly Correctable data error" status. False results will be obtained if this command is issued at any other time (including after a previous REQUEST SYNDROME command).

3-42. Seven words are returned after a REQUEST SYNDROME command, with the following significance:

†*If used following a VERIFY command, no attempt should be made to correct data, since none has been transmitted.*

RETURN WORD 1



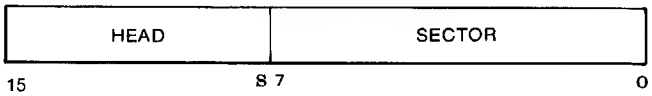
S = Spare track
P = Protected track
D = Defective track
U = Unit

7103-26A

The status may be "Correctable" or "Uncorrectable" (017 or 010 octal) at this point. If uncorrectable, ignore displacement and pattern words. If correctable (017), correction data is available in displacement and pattern words.

RETURN WORD 2

RETURN WORD 3



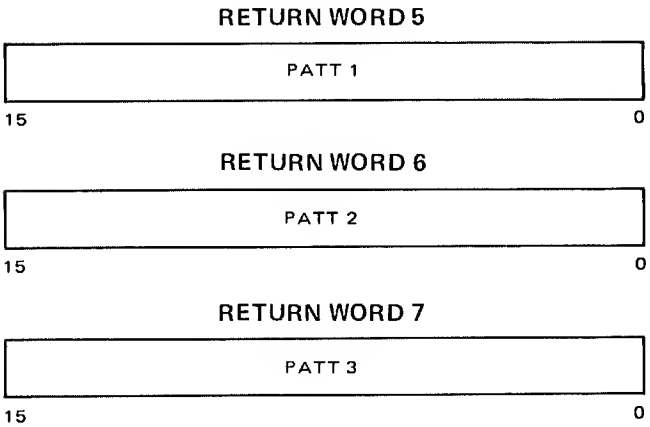
7103-27

Returns two words for cylinder, head, sector addresses in which error occurred.

RETURN WORD 4

7103-28

Displacement indicates the beginning word within the sector where first bit error occurred. The location is given relative to the first data word. The first data word is numbered zero. Thus, to obtain the address of the first word to be corrected, displacement is added to buffer base address of sector (first data word). If displacement number is negative or greater than 125, all or part of the error occurred in the preamble or postamble. The computer should not try to correct errors in these areas, since their contents were not transferred into the computer's memory. If a full sector was not transferred, computer must check the contents to ensure that displacement is within the buffer.

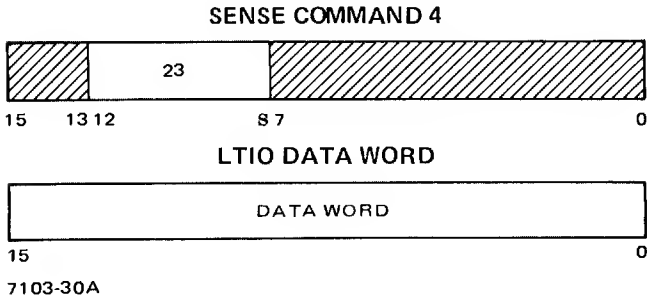


7103-29

Pattern words PATT1, PATT2, and PATT3 are generated by the controller for error correction. These words are "exclusive-or'ed" with the data word errors, beginning with the word indicated by the displacement number. Performance of the "exclusive-or" function of the computer corrects the errors.

3-43. The REQUEST SYNDROME command will complete in less than 700 microseconds. When the process is complete, the controller addresses the next logical sector and waits for a command or until timeout occurs. If the transfer was not complete, the interface may issue a READ without an intervening SEEK or ADDRESS RECORD to continue the transfer. Polling is not resumed when REQUEST SYNDROME is completed.

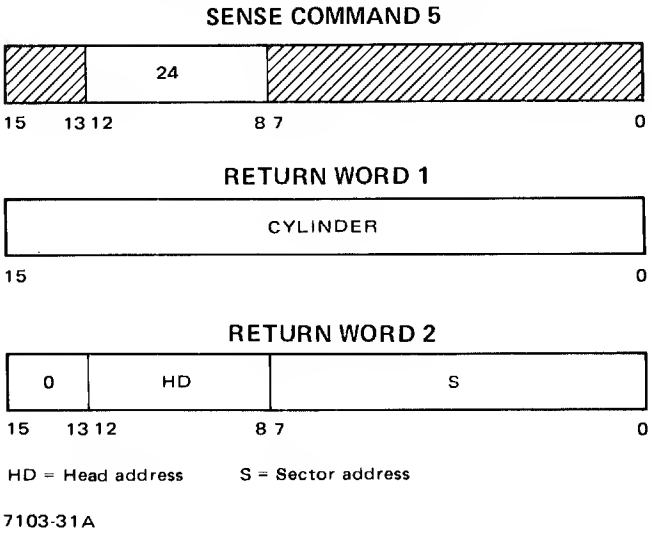
3-44. LOAD TIO REGISTER



7103-30A

3-45. The controller accepts a word of data which is written into the TIO (status) register on the interface by a Write Interface Status Register (WRTIO) order. The controller then transmits Request Service (RQSRV) to the interface and suspends polling. This command is intended as a diagnostic tool for those interfaces which have a TIO register.

3-46. REQUEST DISC ADDRESS



7103-31A

3-47. In response to a REQUEST DISC ADDRESS sense command, the controller returns two words in the order and format of the address words passed in a SEEK command. The words contain the current disc address stored in the controller. This is the address of the current sector if a data error occurred, or the address of the next logical sector if no data error occurred. The command may be used at any time, but it is most useful following a multiple-sector I/O or VERIFY command which aborted with an error. This command allows the operating system to determine where the abort occurred. After completion, the controller transmits Request Service (RQSRV) to the interface and waits for a command or until timeout occurs.

3-48. READ COMMANDS

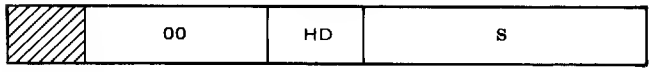
3-49. Read commands transfer information from a disc drive to the computer main storage. On all read commands except "read full sector" the controller examines correction and cyclic code words to check the validity of each record area. For the "cold load read", "read", and "read with offset" commands if the drive unit is available, sparing will occur if necessary and enabled. The controller then begins reading from either (1) the sector last addressed by SEEK, (2) the sector last addressed by ADDRESS RECORD, or (3) the sector following the last sector transferred. This choice depends upon which of these occurred most recently.

3-50. The controller transfers 128 words per sector (138 words for READ FULL SECTOR) until the interface sets End of Data (EOD) or until the controller is unable to continue the transfer due to a drive, interface, or data error, or conditions specified by the File Mask. The controller always processes complete sectors; therefore, normal completion or any errors which occur will be reported at the end of the current sector. EOD can be asserted at any time during a data transfer if only part of a sector is to be read. Sparing will occur at the beginning of a new track if enabled and necessary.

3-51. On normal completion of READ data transfers, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun or data error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to send STINT to the interface. In any case the controller waits for a command from the same interface or for a timeout.

3-52. COLD LOAD READ

READ COMMAND 1



HD = Head address S = Sector address

7103-32

3-53. The COLD LOAD READ is a command to read from cylinder 0 of unit 0 at a specified head and sector address. In operation the controller first checks that drive unit 0 is not busy (i.e., connected to current interface or the hold bit is clear). If busy, it resumes polling until unit 0 is not busy, then executes the COLD LOAD READ command. While waiting for seek completion after issuing a SEEK to unit 0, cylinder 0 and the head and sector specified in the command word, the controller issues the SET FILE MASK control command with Sparing Enabled, Incremental Seek Not Allowed and Surface Mode. The controller then transmits a 0 retry count to the CPU interface and begins reading, starting with the sector and head addressed in the command word.

3-54. READ

READ COMMAND 2

H = Hold bit U = Unit number

7103-33

3-55. In response to a READ command, the controller first checks that the specified drive unit is available, accesses a spare track (if necessary and enabled), then reads data as described in paragraph 3-50.

3-56. READ FULL SECTOR

READ COMMAND 3

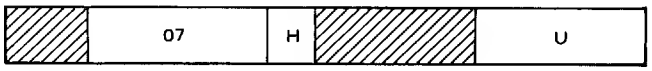
H = Hold bit U = Unit number

7103-34

3-57. In response to a READ FULL SECTOR command the controller first checks that the specified drive unit is available, then transfers 138 words per sector (sync word, cylinder address word, head sector address word, 128 data words, CRC word, and 6 ECC words) to the computer as described in paragraph 3-50. The controller starts the transfer at (1) the cylinder, head, and sector last addressed by a SEEK command, (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command, or (3) the sector following the last sector transferred, whichever occurred most recently. No data error checks are made. Sparing will not occur, either at the start of the command or at the start of a new track. This command is intended for use by diagnostics. It should be used with caution since all address and data error checks are disabled.

3-58. VERIFY

READ COMMAND 4



SECTOR COUNT

H = Hold bit U = Unit number

SCNT = Sector count

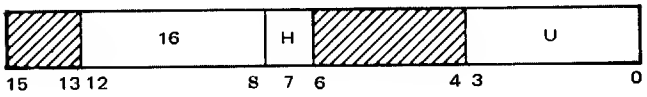
7103-35

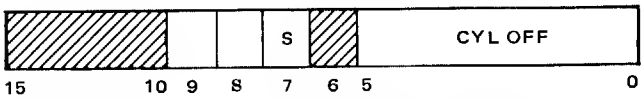
3-59. In response to a VERIFY command, the controller first checks that the specified drive unit is available. If so, the controller requests the sector count word (SCNT) from the interface. SCNT designates how many sectors are to be verified. If SCNT is zero, 65,536 sectors are assumed. The controller then ac-

cesses a spare track (if necessary and sparing is enabled), and reads from the disc *without passing data to the computer.* The controller continues to scan sectors until SCNT has decremented to zero or until the controller is unable to continue due to a drive or data error, or conditions specified by the File Mask (the appropriate error status will be returned as determined by the condition of the controller when the verifying process stops).

3-60. READ WITH OFFSET

READ COMMAND 5





H = Hold bit
U = Unit number

CYL OFF = Cylinder offset magnitude
S = Sign bit (Direction)

7103-36

3-61. The READ WITH OFFSET command performs like a normal read except that before data transfer begins the heads are moved from track center according to an offset parameter word requested by the computer. After fetching the parameter, the controller transmits RQSRV and STDFL to the interface. Dual Channel Port Controller (DCPC) or Direct Memory Access (DMA) should not be activated for the data transfer portion of the command until one or both of these signals are received on the interface.

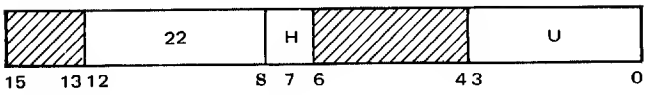
3-62. The controller transmits the cylinder offset value to the selected disc drive. A cylinder offset of zero is on the track center. Offset parameters in the range of +63 to -63 move the heads from track center by incremental distances characteristic of the drive. All offsets are removed after normal command completion or error terminations.

3-63. This command is usually used only in error recovery situations when normal re-reads and REQUEST SYNDROME commands have failed. Since each offset operation requires a minimum of 1.5 milliseconds to complete, the target sector will have passed under the heads by the time the offset is complete, thus requiring an extra rotation of the disc. A similar amount of time is required at the end of the command to restore the heads to track center.

3-64. Spare tracks cannot be read with offset. This is because the offset parameter is sent to the drive before the spare track is accessed, and the seek to the spare track removes the offset.

3-65. READ WITHOUT VERIFY

READ COMMAND 6



H = Hold bit U = Unit number

7103-37

3-66. The READ WITHOUT VERIFY command performs like a normal read, but does not verify a sector before starting to read. Therefore, no address checking or sparing operations occur unless a track boundary is crossed during the operation.

3-67. WRITE COMMANDS

3-68. Write commands transfer information from the computer main storage to the controller for recording on a disc. Except for the WRITE FULL SECTOR command while writing a record on a disc track, the controller appends the preamble and appropriate correction code words to each record area.

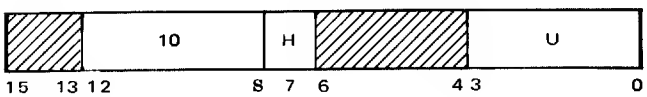
Note: The computer must supply 138 words (all words except the 12-word sync field) during a WRITE FULL SECTOR command.

3-69. The control transfers 128 words per sector (138 words for WRITE FULL SECTOR) until the interface sets End of Data (EOD) or until the controller is unable to continue the transfer due to a drive or interface error, or conditions specified by the File Mask. The controller always processes complete sectors; therefore, normal completion or any errors which occur will be reported at the end of the current sector. EOD can be asserted at any time during a data transfer if only part of a sector is to be written. In this case, the controller will repeatedly write the last transmitted word into the remainder of the sector data field.

3-70. On normal completion of WRITE commands, set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. In any case, the controller then waits for a command from the same interface or for a timeout.

3-71. WRITE

WRITE COMMAND 1



H = Hold bit U = Unit number

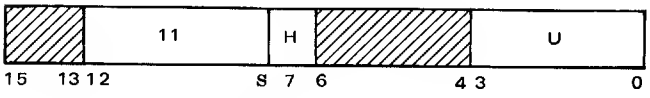
7103-38

3-72. The controller first checks that the specified drive unit is available. If so, sparing will occur if necessary and enabled. The controller then begins writing from either (1) the sector last addressed by SEEK, (2) the sector last addressed by ADDRESS RECORD, or (3) the sector following the last sector transferred. This choice depends upon which of these occurred most recently.

3-73. The operation will be aborted whenever a track is encountered which has been flagged protected (unless the FORMAT switch of the disc drive is set to •), or if the surface is protected by the disc drive PROTECT (READ ONLY) switch(es).

3-74. WRITE FULL SECTOR

WRITE COMMAND 2



H = Hold bit U = Unit number

7103-39

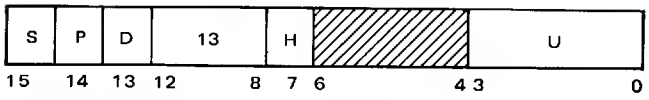
3-75. The WRITE FULL SECTOR command is like a WRITE command except that the computer must pass the sync word, address words, and postamble to the controller in addition to the data field. This command is intended only as a diagnostic tool.

3-76. Using the same procedure as for WRITE, the controller first checks that the specified disc drive is available and then begins writing but without verifying a sector in advance and without accessing a spare track. Then the computer transfers 138 words in the same manner as the 128 words for WRITE except that the controller will request 138 words per sector (sync word, cylinder address, head-sector address, 128 data words, CRC word, and 6 ECC words). The controller starts the transfer at (1) the cylinder, head, and sector last addressed by a SEEK command, (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command, or (3) the sector following the last sector transferred, whichever occurred most recently.

3-77. The operation will be aborted if the FORMAT switch on the disc drive is *off*, or if the surface is protected by the disc drive PROTECT (READ ONLY) switch(es). It is strongly recommended that any multiple sector transfers not cross a track boundary since all address verification and track status checks are off, except when a subsequent track boundary is crossed.

3-78. INITIALIZE

WRITE COMMAND 3



S = Flag track spare
P = Flag track protected
D = Flag track defective
H = Hold bit
U = Unit number

7103-40

3-79. On receipt of the INITIALIZE command word, the controller checks that the surface is not protected by the disc drive PROTECT (READ ONLY) switch(es) and that the FORMAT switch on the disc drive is set to • before executing the command. The controller then begins requesting data from the computer and writes 128 data words on the addressed sector without verifying the preceding sector and without accessing spare tracks. Data transfer is described in paragraph 3-69. Except for not verifying a sector, not accessing a spare track, and the ability to flag tracks using the S, P, and D bits, an INITIALIZE operation is the same as for WRITE.

3-80. Bits 13, 14, and 15 of the INITIALIZE command word flag the track as defective, protected, or spare. Subsequently, when a drive operation is attempted on a track so marked, the status of the track last accessed by that operation will appear in bits 13-15 of a STATUS 1 word. It is the responsibility of the system to ensure that all sectors on a track have the same status.

3-81. If the D bit is set, the track is considered defective and sparing will occur if required and enabled. The only drive operations allowed on a track so marked are READ FULL SECTOR, READ WITHOUT VERIFY, INITIALIZE, and WRITE FULL SECTOR. The latter two will not preserve track status unless specifically directed to do so.

3-82. If the P bit is set, a WRITE operation will only be allowed on that track if the FORMAT switch is set to •. Track status (the state of the S, P, and D bits) will be preserved. An INITIALIZE or WRITE FULL SECTOR command will also only be allowed if the FORMAT switch is set to •, but will not preserve track status unless specifically directed to do so.

3-83. If the S bit is set for a track, a spare track is in active use. Data operations including VERIFY but excepting INITIALIZE, WRITE FULL SECTOR, READ FULL SECTOR, and READ WITHOUT VERIFY will not be allowed on a track so marked unless access is made through its corresponding defective track. INITIALIZE and WRITE FULL SECTOR will not preserve track status unless directed to do so.

3-84. It is strongly recommended that any multiple sector transfers using the INITIALIZE command not cross a track boundary, since all address verification and status checks are off. In addition, a track boundary *must* not be crossed during a multiple sector transfer whenever tracks are being flagged spare or defective since the automatic track sparing algorithm may not work.

THEORY OF OPERATION

SECTION IV

4-1. INTRODUCTION

4-2. This section discusses the functional operation of the controller, first from an overall concept and then each block is segmented and described separately. Included are the microprocessor PCA, device controller PCA, error correct PCA, interfaces between the controller and CPU, interfaces between controller and disc drive, and power supply.

4-3. OVERVIEW OF DISC CONTROLLER

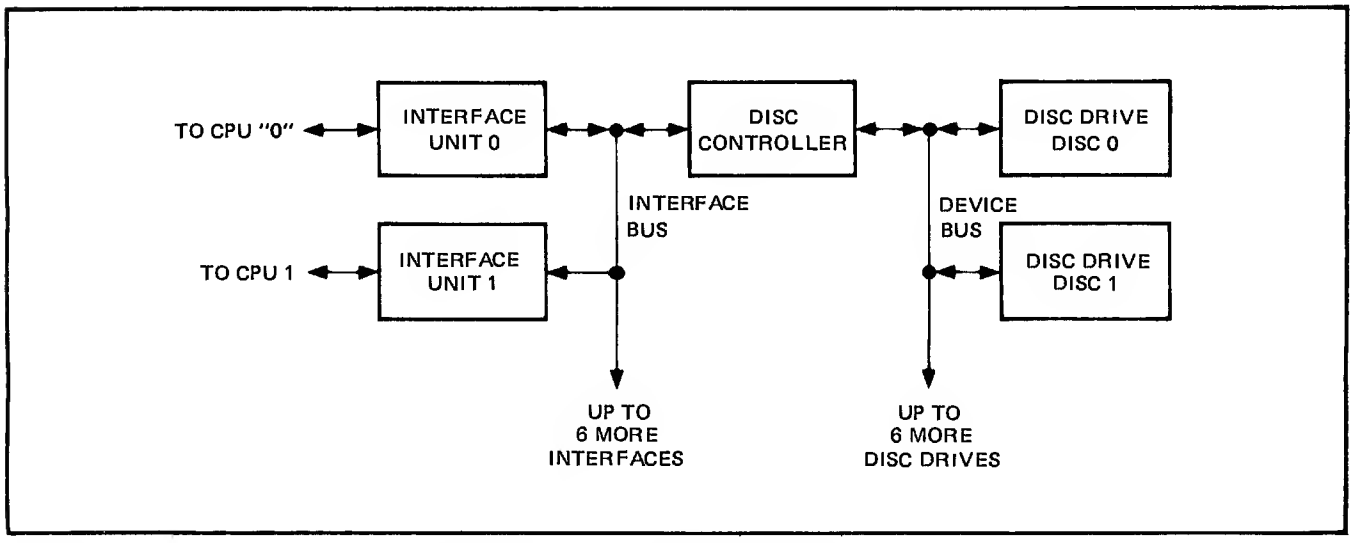
4-4. The controller can access from one to eight disc drives. (See figure 4-1.) Data is transferred to and from the disc at 7.5 Megabits/second, or about 937.5 Kilobytes/second. Multiple CPU interfaces may be connected to the controller. The CPU interface PCA transfers commands from the CPU to the controller. The interface could include data buffering, provisions for different programming methods of sending commands to the controller, logic level differences between the controller and a CPU, and handshake signals and sequences needed by an I/O section of a CPU.

4-5. The functional circuitry (except power supply) of the Model 13037 Disc Controller is contained on three PCA's: the device controller, the microprocessor, and the error correct (ECC/ROM). (See figure 4-2.)

a. The device controller PCA communicates with the CPU interface and the disc drives. It receives input commands and write data from a CPU interface, serializes and formats the data for writing on a selected disc, and separates and de-serializes data from the disc for transmission to the CPU interface. In addition, in the write mode, the device controller encodes the data into a 16-bit pattern for recording in the CRC field of the sector. In the read mode, the device controller re-encodes the data from the disc and compares it with the previously written CRC word. This comparison determines whether or not an error has occurred. A more detailed data integrity check is also made by the ECC/ROM PCA.

b. The microprocessor supervises overall controller operation by addressing and enabling appropriate circuit blocks in response to input commands from the CPU interface. The input commands place the controller into one of four operational categories: control operations, which do not involve transfer of data between the controller and CPU; sense operations, which determine the state of the controller and selected disc drive, and which identify the nature of any errors or unusual conditions that may have occurred; read operations, which transfer data from the disc to the CPU main storage; and write operations, which transfer data from the CPU main storage to the selected disc. The microcode instructions for specific operations within each category are stored in a 24 bit by 1024 word ROM located on the ECC/ROM board.

c. In the write mode, the ECC/ROM encodes the data to be written on the disc into the six-word Error Correction Code (ECC) for recording in the ECC



7103-41A

Figure 4-1. Disc Drive Subsystem Block Diagram

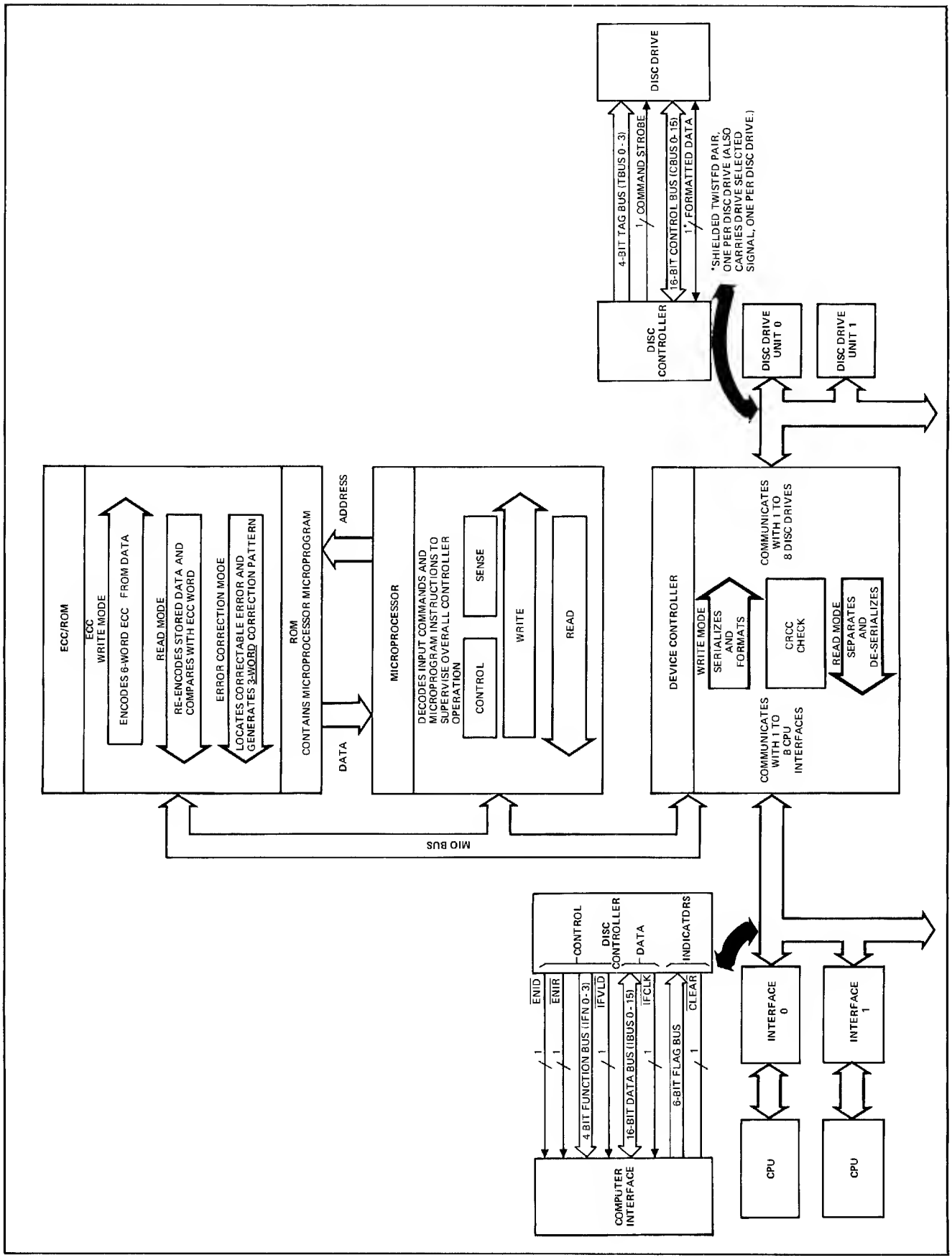


Figure 4-2. Controller Overall Functional Block Diagram

field of the sector postamble. In the read mode, the ECC/ROM re-encodes the data from the disc and compares it with the previously written ECC information. This comparison determines whether the sector of data has been transferred to the CPU without error, with an uncorrectable error, or with a possibly correctable error. A possibly correctable error is where one or more errors are contained within a single 32-bit burst with no other errors detected in the sector. An uncorrectable error is where two or more errors occur with a bit separation greater than 32 bits. When commanded by the CPU interface (Request Syndrome), the ECC circuitry further manipulates the data to determine if the error is really correctable, and where in the sector the error burst is located. In addition, the ECC circuitry generates a four-word data pattern to tell the CPU where the error burst is located, and a three-word correction pattern which the CPU can "exclusive-or" with the previously supplied data to correct the error.

4-6. FUNCTIONAL DESCRIPTION

4-7. The execution of commands for data transfer requires the controller to perform numerous internal operations. When data supplied by the computer is to be written by the disc drive, the control sequence of the write operation transfers the addresses designating disc drive, head and sector, and cylinder; checks disc-drive seek ending address; checks for proper sector format (including address field and data field); activates parallel-to-serial conversion of data words; issues check words and error words; and monitors the write operation until it is completed. When data is to be transferred to the computer from the disc for a read operation, the sequence is as follows: transfer of all required addresses; check disc-drive seek ending location; serial-to-parallel conversion of data words; check for data errors; and monitor the read operation until completed.

4-8. GENERAL DESCRIPTION

4-9. The microprocessor PCA supervises the overall controller operation by implementing instructions from the microprogram read from a read-only-memory (ROM). As shown in figure 4-12, the microprocessor consists of the following functional blocks:

a. The internal 30 MHz clock logic and crystal (not shown) that controls the overall controller timing.

b. The 12-bit ROM address register (RAR) logic that specifies the next instruction to be read from the ROM.

c. The ROM output register (ROR) logic which holds and distributes 24-bit microcode instruction words received from the ROM.

d. Decoding logic to decode the contents of the ROR.

e. Condition select logic to control branching within the microprogram.

f. Eight 16-bit general-purpose registers (GPR) (A0-A3 and B0-B3) used for storage and I/O of microprogrammable data.

g. The arithmetic logic unit (ALU) manipulates immediate data (stored in the microinstruction itself) and data stored in the eight GPR's as directed by the microprogram.

h. Rotate-shift logic (shifter) which can shift or rotate data one bit to the right or left or exchange upper and lower bytes before storing the result of a computation into a GPR.

i. The three-level microcode subroutine stack which provides storage for return addresses so that the main microprogram can resume at the correct place after a subroutine has completed.

4-10. CONTROLLER INSTRUCTIONS

4-11. All data and command communication conducted between the microprocessor PCA, error correct PCA, and device controller PCA is routed via the microprocessor input/output (MIO) bus. The MIO bus is used for input, output, and as the return path to the registers. Input data through the MIO bus is loaded into the selected registers. As directed by the microprogram, the data to be processed goes via the A and B buses to the ALU, and then back through the MIO bus after processing. The A bus is driven by the immediate operand field of the microcode instruction or registers A0 through A3. The B bus is driven by B0 through B3 registers. The microprocessor microcode instruction set contains arithmetic and logical instructions and conditional branching microinstructions controlling the ALU and rotate/shift logic. Seventeen external flag lines and six microprocessor status indicators, which permit selective branching on condition, are also provided. The A and B registers are divided into upper and lower bytes. Data operations can be performed using the upper byte, lower byte, or the full 16-bit word. Five destination/source bits are provided to select the source or destination desired when executing an input/output instruction.

4-12. The microprocessor PCA shifter provides rotate and shift logic which outputs to the MIO bus. Three-state logic is used. Shift and pass instructions in the microprocessor can be used with upper or lower bytes, or full words. Rotate and swap instructions require full words only.

4-13. The ROM address register (RAR) addresses the ROM and the ROM output register (ROR) receives the ROM microcode instructions. The majority of ROR field readout in the microprocessor goes to the decode and control logic. The exception is the Immediate Operand field which is passed to the address gating and ALU.

4-14. DATA TRANSFER. The device controller PCA is used as the input/output section of the controller. The microprogram controls the clocks and enables of the device controller for the proper transferring of data between a computer and disc drive. The format in which address and data fields are written on the disc is controlled by a data formatter. A sector compare pulse from the disc drive activates the formatter. By counting bits and 16-bit words, and by enabling data writing at prescribed times, each sector is written in the format shown in figure 3-2.

4-15. Serial data from the output of the Serial-Deserializer (SERDES) is fed to Cyclic Redundancy Check Code (CRCC) and Error Correction Code (ECC) generators. The bit pattern of the 16-bit CRCC word is a function of the sync word, address words, and data field bit patterns and the Boolean equation of the CRCC generator. The ECC words are generated as a function of the sync word, address words, data, and CRCC fields.

4-16. Serial data read from the disc drive is applied to a phase-locked loop in the data separator. Because slight variations in the rotational speed of disc drives causes the frequency of the clock information contained in the read data to vary, the phase-locked loop includes a voltage-controlled oscillator that provides the frequency flexibility required to compensate for these variations. The phase-locked loop produces a nominal output of 7.5 MHz, the precise frequency of the data when written. The combination of the phase-locked loop output and the read data input is used to generate a data clock which clocks the serial data bits at the frequency they are actually coming from the disc drive. Separate data is routed to the SERDES, the CRCC generator, and the ECC generator. The CRCC and ECC generators process the read data and corresponding check words at the end of each data field and determine if a data error has occurred. If a possibly correctable data error is reported and, in response, a REQUEST SYNDROME command is received, the controller will attempt to provide the information required to correct the error.

4-17. DISC ADDRESS. The random-access-memory (RAM) is a 64-bit (16 × 4) read/write memory device used as a scratch pad memory by the controller. Since the controller has the capability to be connected with eight interfaces and eight disc drives, the RAM is used to store the associated disc drive and interface numbers. A "hold" bit sent with a command from the interface, is also stored. The RAM Address Register is used to address a particular memory location in the RAM.

4-18. CONTROLLER POLLING

4-19. The controller treats each of the CPU ports (interfaces) as a peripheral device. A polling flowchart is shown in figure 4-3. In operation, each CPU interface port in a serial sequence is connected to the controller and checked for a command word requesting service. If there is no command, the port is disconnected and the disc drive attention bits are checked simultaneously. If no disc drive wants attention, the next port in sequence is polled, and so forth until a port command or an attention bit is detected. When a command word at a port is recognized by the controller, it is decoded and sent to the command processor where it is interpreted as requiring disc drive access or not and whether or not a "hold" bit check is needed. Disc drive unit numbers in such commands access the RAM location corresponding to that unit and check whether or not the "hold" bit in that RAM entry was previously set. If "hold" is set and the port number stored in that location matches the current requesting port number, the command operation continues. If "hold" is set and the port number stored in that location does not match the requesting port number, the controller will resume polling. The offending command is buffered on the interface and will be retried the next time that port is polled. If the "hold bit" is clear or if the port numbers match, the "hold bit" and the port number will be updated in the RAM according to the "hold" field of the requesting command.

4-20. If a disc drive interrupt request (attention bit true) is noted during the poll sequence, the port number stored in the RAM location corresponding to the drive unit is retrieved. The poll is suspended and the port last using that disc drive is interrupted. The controller then awaits a command from that port.

4-21. Several commands leave information (status of some type, record address, etc.) in the controller. Because storage in both the port (interface) and the controller is limited, to avoid destroying the information the controller suspends the poll and remains connected to the port issuing the command. It is up to the port (interface) to retrieve the information and ultimately issue a command that releases the controller, allowing it to resume its polling sequence. Following all commands, except the END command, the controller starts a 1.8 second timer. If the port does not respond with another command during that time period, it is disconnected and polling resumes. The port is disconnected by any one of the following: an explicit END command, an unsuccessful attempt to access a "hold" drive, a timeout, or the execution of a SEEK or RECALIBRATE command. The port remains connected at all other times, including after a SEEK or RECALIBRATE command is completed. If a port is disconnected by a timeout, all hold bits set by that port are cleared.

4-22. Whenever the poll sequence is resumed, polling continues with the port that would have been connected next regardless of the fact that the controller may have processed an attention interrupt in between sequencing. Therefore, the sequence is never broken.

4-23. DETAILED DESCRIPTION

4-24. The following paragraphs give a detailed description of the microprocessor PCA, device controller

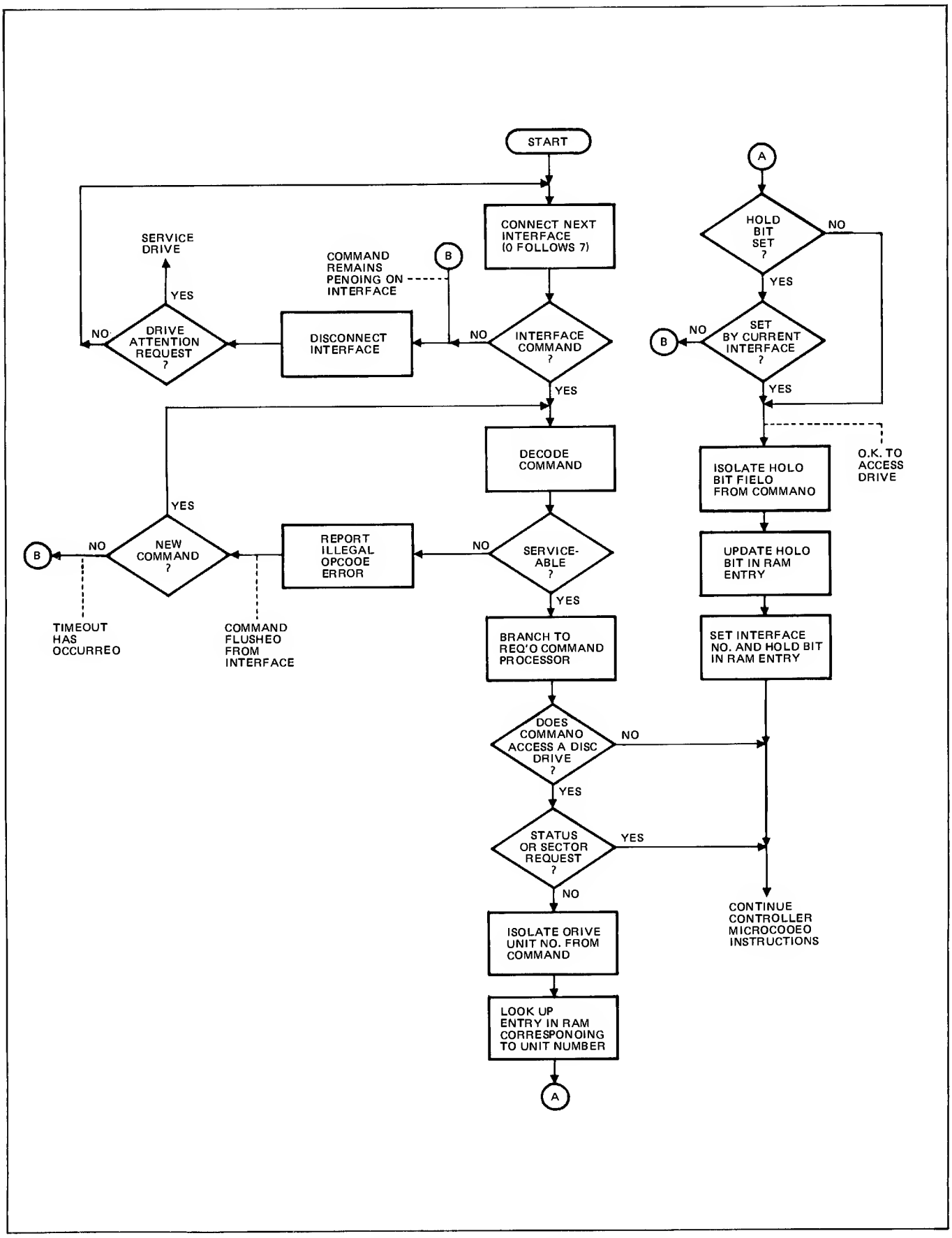


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Figure 4-3. CPU Interface Port Polling Flowchart

PCA, error correct PCA, interfaces, and power supply. Refer to figure 4-12 for the following descriptions.

4-25. MICROPROCESSOR PCA

4-26. The microprocessor PCA functional block diagram is shown in figure 4-12. The left half is instruction sequencing logic and the right half is the registers and arithmetic and logic modules. All microinstructions are contained in the ROM. The command decoding block uses the current instruction to create control signals which operate the various sections of the microprocessor. The ROM Address Register (RAR) contains the address of the next instruction in the ROM. This address is one greater than the previous address if a branch is not being executed. If a branch is being executed, the address gating network selects the proper branch address from one of four possible sources: the subroutine stack, an external address, the T register, or the immediate field of a branch instruction.

4-27. The condition select block tests a flag and sets the Condition Code Bit (CCB). The branch select logic looks at the CCB to decide if the branch is to succeed or fail. It also determines what type of branch is to occur.

4-28. The right part of figure 4-12 microprocessor block shows the four A and four B registers which may act as inputs for the ALU. Note that an 8-bit *immediate operand* may replace an A register in some instructions. The ALU output is buffered in the T register. Following this, the shifter rotates, shifts, or swaps bytes, putting the result on the MIO bus. This result is then directed to either an A or B register or to an external destination. The processor status register (PSR) latches six ALU and T register conditions and makes them available to the conditional branch test circuitry. (See paragraph 4-32.)

4-29. ARITHMETIC LOGIC UNIT (ALU). The ALU performs all of the functions listed below. ROM bits 16 through 20 and 14 in arithmetic and I/O microcode instructions specify which operation is to be performed. All operations may be performed on a 16-bit (full word) or 8-bit (byte) basis. An exception occurs where an operation involving an immediate operand can be performed on an upper or lower byte only. ALU and T register status is available after each arithmetic instruction and is held in the processor status register (PSR). Binary operations (marked *) must be performed on data in an A register (or immediate operand) and a B register. Two registers of the same type are not allowed. The result may go in any register. Note that subtraction is always "A minus B". The functions are the following:

PLUS*	INCLUSIVE OR*
MINUS*	EXCLUSIVE OR*
PASS	COMPLEMENT (one's complement)
INCREMENT (A-reg only)	LOGICAL AND*
DECREMENT (A-reg only)	

4-30. BUSES. The ALU is driven by the A and B buses, each of which connects to four 16-bit registers. The A bus also connects to the 8-bit *immediate operand* field of the ROR. It should be noted that all binary immediate operations are with B registers. All information on these buses is ground true. The MIO bus is a three-state bus which connects the output of the ALU shifter to the registers. As shown in figure 4-12, this bus is also connected to the device controller and error corrector functional blocks. Information on this bus is ground true.

4-31. A AND B REGISTERS. Eight 16-bit registers are implemented. Four registers (A0-A3) drive the A bus and four (B0-B3) drive the B bus. All are fed from the MIO bus. Microcode instructions may affect only the upper or the lower byte of these registers and, in some cases, may affect the entire 16 bits.

4-32. CONDITIONS. Seventeen external flags and six processor status indicators are available for use in conditional branches. They are positive true. The flags indicate conditions in the device controller PCA, error correct PCA, or CPU interface. Processor status is recorded during each arithmetic/logic instruction in the PSR and is available until the next arithmetic instruction. Process status includes the following:

EQUAL	available after a subtract instruction. Signifies that contents of selected A and B registers are equal.
UOVER	signifies overflow (carry) out of ALU upper byte.
LOVER	indicates carry out of lower byte of ALU.
TNZRO	indicates that contents of T register are not zero.
TMSB	most significant bit (MSB) of T register is true.
TLSB	least significant bit (LSB) of T register is true.

4-33. SET CONDITION CODE. A Set Condition Code (SCC) instruction should be executed before a branch to clock the selected condition (external flag or processor status) into the condition code bit (CCB). The following branch will depend on the value set in the CCB by the last SCC instruction. If the CCB is false, the branch will not succeed and the microprogram continues at the next address. Any unsuccessful branch sets the CCB true to allow subsequent branching. Any SCC instruction can be coded with RS to reverse the sense of any flag or PSR bit. For example, "CC = TNZRO,RS" would set the CCB true if the T register contains zero.

4-34. SUBROUTINE STACK. The subroutine stack is a three-level last-in-first-out (LIFO) or push-down stack. This register can store up to three microcode return addresses which allows three levels of subroutine nesting. With this implementation, the main microprogram can be diverted to a subroutine and return to the correct place after the subroutine is complete.

4-35. T REGISTER. The T register stores the results of an ALU calculation. An indirect branch loads the contents of the T register into the RAR.

4-36. SHIFTER. The shifter receives the ALU output through the T register, does the necessary shifting, and outputs the result to the MIO bus. Allowable shifts are: shift left, shift right, rotate left, rotate right, swap bytes and pass (unchanged). All shifts are valid on full word (16-bit) operations. The only shifts valid for byte operations are shift left, shift right and pass. The shifter is disabled (pass only) whenever an immediate operand is used.

4-37. CLOCKS. The controller runs on a crystal-controlled 30-MHz clock. The output of the clock is fed into a ring counter which generates six phases labeled T0 through T5. Each microcode instruction is executed in 200 nanoseconds.

4-38. ROM ADDRESS REGISTER AND ADDRESS GATING. The ROM address register (RAR) is a 12-bit counter register which addresses the ROM. Normally, the next instruction is the current address plus one, so the RAR is incremented during each instruction. The RAR address gating provides for different types of branching in the microcode instructions. In a branch, one of four different address sources is loaded into the RAR. This address may come from the BRANCH ADDRESS field of the ROM microinstruction word, the subroutine stack, T register, or an external source (not shown) such as a service device attached to the controller.

4-39. READ ONLY MEMORY (ROM). The microprocessor ROM consists of twenty-four 256 × 4 bit chips. These ROM's are organized as four banks (horizontal rows) of six ROM's per bank. This configuration gives an instruction word length of 24 bits and allows 1024 microcode instructions to be stored.

4-40. DEVICE CONTROLLER PCA

4-41. The device controller PCA contains circuitry which serializes and deserializes (SERDES) data as it is transmitted/received to/from the CPU interface as 16-bit words. The functional block also has a data formatter/separator which translates between non-return-to-zero (NRZ) coded data and time delay modulated data. The device controller PCA has a cyclic redundancy code check (CRCC) generator for checking the validity and integrity of data transmitted/received with the disc drive. A RAM is used as a changeable look-up table of interconnections between the eight disc drives and CPU interfaces (see paragraph 4-51). The device controller also contains interfaces, registers, drivers, and receivers that support the tag and control buses for the disc drive. It also contains interfaces, registers, drivers, and receivers that support the function and data buses for the CPU interface.

4-42. Basically, all connections made external to the controller (i.e., the CPU interface and disc drive) are made through the device controller PCA. The device controller PCA and microprocessor PCA are linked by the bidirectional 16-bit MIO bus, five external address lines, and several flags. All registers, drivers, and receivers are connected to the MIO bus and are assigned one of 32 external addresses.

4-43. SERIAL-DESERIALIZER (SERDES). The SERDES converts parallel-to-serial and serial-to-parallel data between the CPU interface and disc drive. A 16-bit word is received in parallel from the CPU interface and is shifted out serially to the formatter-separator. From the formatter-separator, the data is transmitted serially to the disc drive. When reading from the disc drive, data is received serially by the formatter-separator. The serial data is clocked from the formatter-separator to SERDES. When 16 bits have accumulated in the serial-to-parallel input buffer of SERDES, the data word is transmitted in parallel to the CPU interface.

4-44. DATA FORMATTER-SEPARATOR. The data formatter-separator is the final data output to and from the disc drive. The following discussion is divided into write and read operations. Figure 4-4 is an overall block diagram of the data formatter-separator.

4-45. The encoded write and read data is transmitted in a common shielded twisted pair transmission line between the controller and disc drive. Multiple disc drives are data cabled in a "star" configuration with each disc drive connected directly to a data port on the device controller. There are eight data ports on the device controller. These ports are non-dedicated. That is, any disc drive (logical unit) may be connected to any port. The line driver or receiver for each port is enabled by unit select being returned with logical low state from a selected disc drive.

4-46. Data Formatter. When the data formatter is enabled by a write command from an internal control word and a sector compare is received from a disc drive (formatter-separator control), the write clock generator clocks the data to be written through a four-bit shift

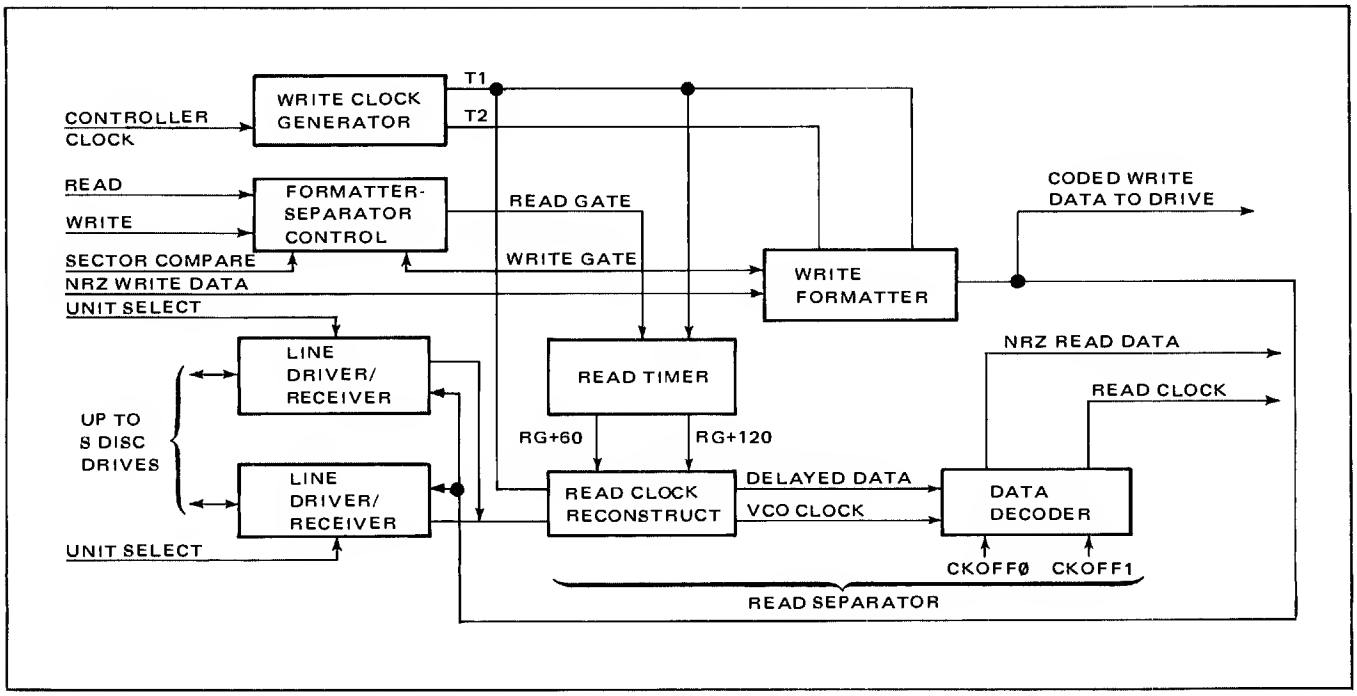

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Figure 4-4. Data Formatter-Separator Block Diagram

register. The data is clocked from SERDES at a 7.5-MHz rate derived from the 30 MHZ clock on the microprocessor. As the data passes through the shift register, it is NRZ encoded and precorrected before being transmitted to the disc drive. Modified frequency modulation (MFM) coding is implemented using the following rules: (1) a transition is made in the middle of a "one" bit cell, and (2) a transition is made between two adjacent "zero" bit cells.

4-47. The encoding is accomplished by sensing the pattern in the shift register and passing an appropriately phased write clock pulse where a transition should be made. The precorrection function decreases the effects of pulse crowding during a read operation. In summary, patterns in the shift register are detected to select an amount of time delay for each encoded write pulse. Pulses receiving no precorrection are nominally delayed and pulses to be advanced or retarded receive less or greater delay, respectively. Pulses preceded by a two-bit cell gap and followed by a one-bit cell gap are advanced. Pulses preceded by a one-bit cell gap and followed by a two-bit cell gap are delayed.

4-48. Data Separator. When the data separator is enabled by a read command from an internal control word and a sector compare is received from a disc drive (formatter-separator control), a timing sequence is initiated. The timing is done at a bit cell rate and referenced to the controller clock (write clock generation and read timer). For 60 bit cells, the incoming data is ignored and the data separator phase-locked-loop (PLL) (read clock reconstruct) is locked to the controller clock which is the normal state for other than read operations. After the 60th bit cell interval, the signal input of the PLL is switched to the incoming data and the PLL locks to the zero field of the sector. After 120 bit cells have been counted, the PLL is assumed locked to the zero field and is enabled to track and retain lock on data. The PLL then outputs a data clock to the data decoder. After the 120th bit cell interval, the data decoder is enabled and will detect "ones" in the data stream. The first "one" to be detected is the first bit of the sync word. With detection of the sync bit, all following data and clock are outputted to the SERDES.

4-49. CYCLIC REDUNDANCY CHECK CODE (CRCC). During a write operation, the serial data is received simultaneously by the CRCC, the data formatter and the error correct PCA. The CRCC has a 16-bit shift register which operates in a load mode while data is being written on the disc. Its outputs and inputs are interconnected with three exclusive "or" gates in such a way that data is shifted with feedback on each data clock. At the end of the 128 word data field of each sector, the shift register will contain the 16-bit Cyclic Redundancy Check (CRC) word. Next the CRCC shift registers switch from the load to the shift mode so that the next 16 data clocks shift the CRC word out to the error correct PCA and the data formatter for writing on the disc, directly following the data field.

4-50. During a read operation from the disc while the data is being deserialized in SERDES, it is also being shifted into the CRCC shift register (load mode). The shifting is stopped within the shift register when the last bit of the CRC word (following the data) is received. With the CRC word in this "hold" state, circuitry within the CRCC acts as a 16-bit input "or" gate which "or's" together each bit of the CRC word. If any bit is not zero,

there is an error in the sector and a CRC error flag is generated.

4-51. RANDOM ACCESS MEMORY (RAM). To implement the multiple CPU interface communication ability of the controller, a 16-word by 4-bit (16 × 4) RAM is used on the device controller PCA. The RAM correlates each disc drive (up to 8) with the last CPU to access it. The RAM also contains hold bits that indicate whether or not each disc drive may be accessed by a CPU interface other than the last one to access it. The RAM hold bit implements the overlapping seek by multiple CPU feature.

4-52. Figure 4-5 is a diagram of the RAM which maps the disc drive unit number (same as the RAM word number for numbers 0 through 7) into the word number of the CPU interface which last accessed that disc drive. Word 15 contains the word number of the interface last polled to see if a command was pending. Word 14 contains the word number of the interface currently connected to the controller. Word 13 is a sector counter used by the microprogram. Word 12 contains a disc drive type word, four encoded bits returned from the disc drive, which allow the controller to determine the number of heads and the number of sectors per track. Bit 3 of word 11, if true, indicates that the Platter Protect switch for the current surface or the Read Only switch for the disc pack is enabled, thereby prohibiting writing of any kind. Bit 2, if true, indicates that the format switch is enabled to override. All information is stored ground true.

4-53. RAM ADDRESS REGISTER. The RAM address register addresses a particular word in RAM for reading or writing in that cell.

4-54. CONTROLLER/CPU INTERFACE

4-55. The logical and physical interface provides the means for the computer I/O hardware to communicate with the controller. The CPU interface must map from the computer I/O signals to those described in the following paragraphs. In general, the CPU interface acts on orders from the CPU and from the controller. It is considered a slave to the controller in that the CPU I/O functions do not directly affect the controller, but are acted upon by the controller only after the controller interrogates the CPU interface. See figure 4-6 for a block diagram of the CPU interface with the controller. It consists of the following groups of lines: interface control signals, data bus, flags from interface and function bus. Table 4-1 contains a summary of the function bus commands including octal codes and data bus contents. Table 4-2 describes the CPU interface to controller interface functions in more detail.

4-56. CONTROLLER/DISC DRIVE

4-57. As shown in figure 4-7, the controller/disc drive has the following groups of lines:

a. Tag Bus — Four lines specifying what function is to be performed. Table 4-3 is a summary of the tag bus functions including the octal code, operation, and relation to the control bus.

b. Control Bus — Sixteen bidirectional lines containing additional command information (e.g., cylinder address, status). For details, refer to the applicable disc drive installation and service manual. Table 4-4 is a summary of the control bus functions showing the relationship of a function to a specific bus line.

c. Command Strobe — Validates all tag bus functions.

d. Formatted Data — A bidirectional line transmitting bit formatted data between the controller and disc drive.

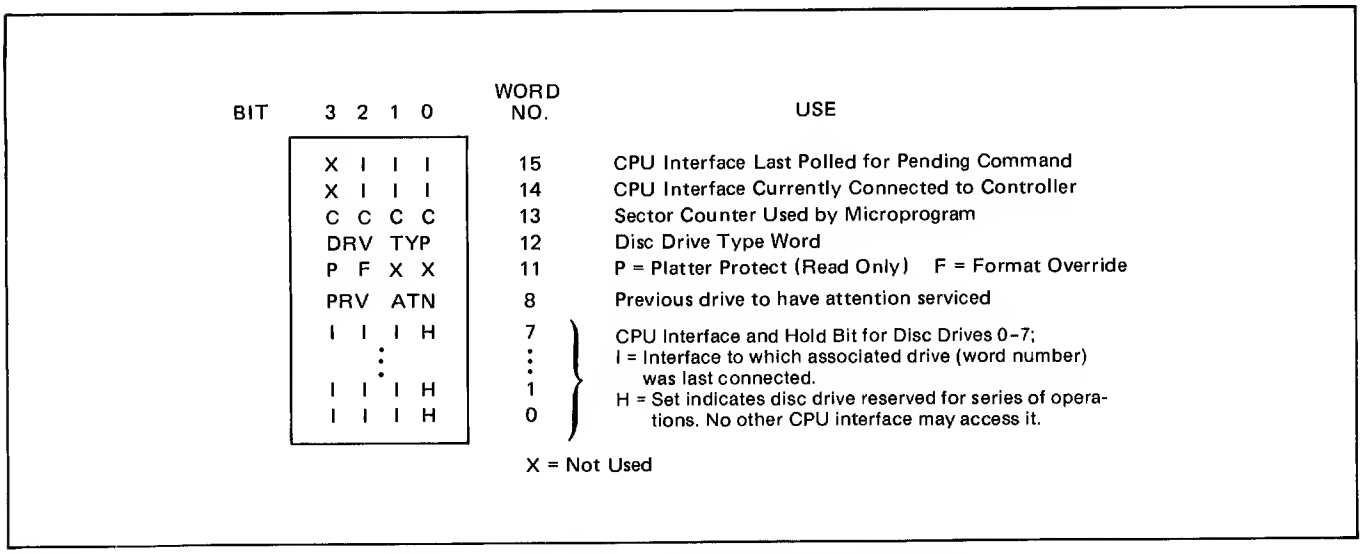

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Figure 4-5. Diagram of Device Controller PCA RAM

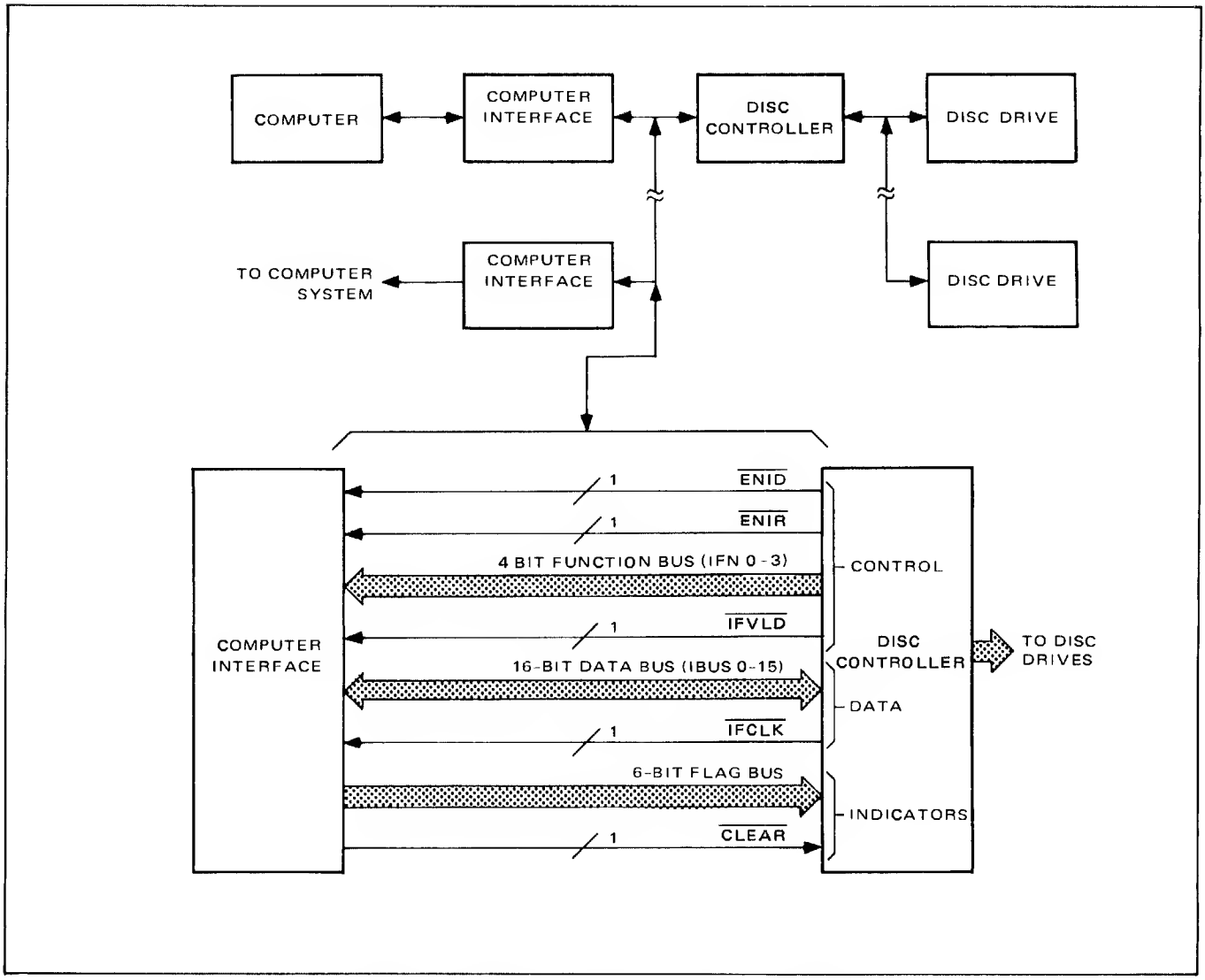

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Figure 4-6. CPU Interface to Controller Interface

Table 4-1. Function Bus Summary

FUNCTION BUS (0-3)	MNEMONIC	FUNCTION DESCRIPTION	DATA BUS CONTENTS
00	STINT	Set Interrupt Request	
01	STDFL	Set Data Flag	
02	IFPRF	Pre-fetch Command	Command Word
03	SELIF	Select Interface	Interface Address
04	SRTRY	Set Retry Counter	Retry Count
05	DVEND	Device End (Set JMP MET)	
06		(Reserved)	
07	RQSRV	Request Service	
10		(Reserved)	
11	DSCIF	Disconnect Interface	
12	WRTIO	Write TIO	Status-1
13	IFOUT	Data Out (Write to Disc)	Data
14	IFIN	Data In (Read from Disc)	Data
15	IFGTC	Get Command	Command Word
16	BUSY	Set/Clear Controller Busy Bit	Busy Status
17		(Reserved)	

Table 4-2. CPU Interface to Controller Interface Signals

INTERFACE CONTROL SIGNALS AND DATA BUS

$\overline{\text{Clear}}$
Hard clear on controller logic.

Data Bus (IBUS 0-15)
Bidirectional 16-bit bus used to transmit commands, data, status, and addresses between controller and CPU interface. Data is validated by IFCLK.

$\overline{\text{ENID}}$ (Enable Interface Drivers)
CPU interface must be selected. Enables data bus drivers on CPU interface.

$\overline{\text{ENIR}}$ (Enable Interface Receivers)
Enables data bus receivers on CPU interface.

Function Bus (IFN 0-3)
Four bit bus validated by IFVLD. Transmits CPU interface functions from controller.

$\overline{\text{IFCLK}}$ (Interface Clock)
Validates word transfers on data bus while IFIN, IFGTC, IFOUT, or WRTIO is true. Trailing edge must be used. (When IFOUT is true, the controller reads data at the leading edge.)

$\overline{\text{IFVLD}}$ (Interface Function Valid)
Validates function on function bus. A function is valid only if this line is true.

FLAGS FROM INTERFACE

Flags are gated out by a CPU interface whose select bit is set.

$\overline{\text{CMRDY}}$ (Command Ready)
True if a command is present in command register. Cleared by IFGTC.

$\overline{\text{DTRDY}}$ (Data Ready)
True if data is present in data buffer. Cleared when data buffer is emptied.

$\overline{\text{EOD}}$ (End of Data)
True if CPU interface has completed a block transfer and data buffer is empty. Not set during data chaining until entire transfer is complete. Cleared when next command is fetched by controller. Note that controller may continue to fetch from data buffer after EOD is set while completing a sector transfer. Therefore, the next command may not be prefetched into data buffer.

$\overline{\text{OVRUN}}$ (Read Overrun)
True if data buffer is full and controller tries to overwrite or data buffer is empty and CPU attempts to fetch. Setting is prohibited by EOD. Cleared when next command is fetched by controller. (Write Overrun is detected by the controller whenever the data buffer is empty and controller attempts to fetch unless EOD is also set.)

$\overline{\text{XFRNG}}$ (Transfer No Good)
False unless the CPU interface detects an error condition (other than overrun) which prohibits transfer of data. Cleared by STINT.

$\overline{\text{INTOK}}$ (Interrupt OK)
True if CPU interface can be interrupted by a disc drive attention request. Other interrupt conditions do not examine this flag.

FUNCTION BUS ORDERS

Note: Orders listed are validated by IFVLD. All edge validations are by trailing edge. The number immediately following the mnemonic is the octal code for that order. Table 4-1 contains a summary of the function bus orders which includes the function bus octal code, mnemonic, mnemonic function description, and the data bus contents.

BUSY (16)
Interface must be selected. ENIR is true. Clocks bit 0 of data bus into a bit on CPU interface which, when bit 0 is high, signifies that controller has accepted a command and is executing it and that requested disc drive (if any) is available. (Bit 0 low = not busy.)

Table 4-2. CPU Interface to Controller Interface Signals (continued)

$\overline{\text{DSCIF}}$ (11) (Disconnect Interface)
All CPU interfaces respond. Used to clear CPU interface select bit. When select bit is false, CPU interface will not respond to select-required commands, or gate its flags or data bus out to the controller.

$\overline{\text{DVEND}}$ (05) (Device End)
CPU interface must be selected. Transmitted by controller to terminate an operation it considers retryable (correctable or uncorrectable data error on read operations, overrun on any data operation).

$\overline{\text{IFIN}}$ (14) (Data In, Controller to CPU Interface)
CPU interface must be selected. ENIR is true. Enables transfers into CPU from controller. While IFIN is true, trailing edge of IFCLK validates individual word transfers. This function is used for all transfers into the CPU.

$\overline{\text{IFGTC}}$ (15) (Get Command from CPU Interface)
CPU interface must be selected. ENID is true. Used to gate contents of CPU interface command register onto data bus. Clears CMRDY flag.

$\overline{\text{IFOUT}}$ (13) (Data Out, CPU Interface to Controller)
CPU interface must be selected. ENID is true. Gates CPU interface data buffer onto data bus. (Data is accepted by controller at leading edge of IFCLK.) Transfer validation is indicated by trailing edge of IFCLK. Used in all word fetches to controller except command fetch which uses IFGTC.

$\overline{\text{IFPRF}}$ (02) (Pre-Fetch Command from Interface)
CPU interface must be selected. ENID is true. Gates contents of command register on CPU interface onto data bus as in IFGTC, but does not clear CMRDY flag or otherwise alter CPU interface.

$\overline{\text{RQSRV}}$ (07) (Request Service)
CPU interface must be selected. Sets service request explicitly at end of any block transfer (in or out) involving more than command word (e.g., SEEK, READ, STATUS, etc.). While a block transfer is in progress, CPU interface may not fetch next command unless it goes to a buffer other than data buffer; RQSRV signals CPU interface that controller has finished with its block transfer and it is all right to fetch next command.

$\overline{\text{SELIF}}$ (03) (Select Interface)
CPU interface need not be selected. ENIR is true. A three-bit address is present on data bus (0-2). If it matches jumpered address on CPU interface, CPU interface uses IFVLD to set its select bit. When select bit is true CPU interface responds to select-required commands, responds to ENID, and gates its flags to controller.

$\overline{\text{SRTRY}}$ (04) (Set Retry Counter)
CPU interface must be selected. ENIR is true. One byte of mode control data is present on data bus (0-7). Data bus (0-3) is interpreted by controller and should be ignored by CPU interface. Data bus (4-7) is for use by CPU interface (e.g., as a retry counter setting). The byte is an image of lower byte passed in a SET FILE MASK controller instruction.

$\overline{\text{STDFL}}$ (01) (Set Data Flag)
CPU interface must be selected. Sets a bit on CPU interface as follows:

To request direct transfer of a single word (SEEK, ADDRESS RECORD, STATUS, REQUEST SYNDROME, VERIFY, READ WITH OFFSET, REQUEST SECTOR, LOAD TIO REGISTER, REQUEST DISC ADDRESS).

When a data operation is complete (COLD LOAD READ, READ, READ FULL SECTOR, VERIFY, WRITE, WRITE FULL SECTOR, INITIALIZE, READ WITH OFFSET, READ WITHOUT VERIFY).

To signal completion of a single-transaction command (SET FILE MASK, WAKEUP, CLEAR RECALIBRATE).

$\overline{\text{STINT}}$ (00) (Set Interrupt)
CPU interface must be selected. Sets interrupt request bit on CPU interface when controller discovers an error condition or when a disc drive is requesting attention.

$\overline{\text{WRTIO}}$ (12) (Write TIO)
CPU must be selected. ENIR is true. Data bus (0-15) contains controller status to be clocked into a CPU-testable status register.

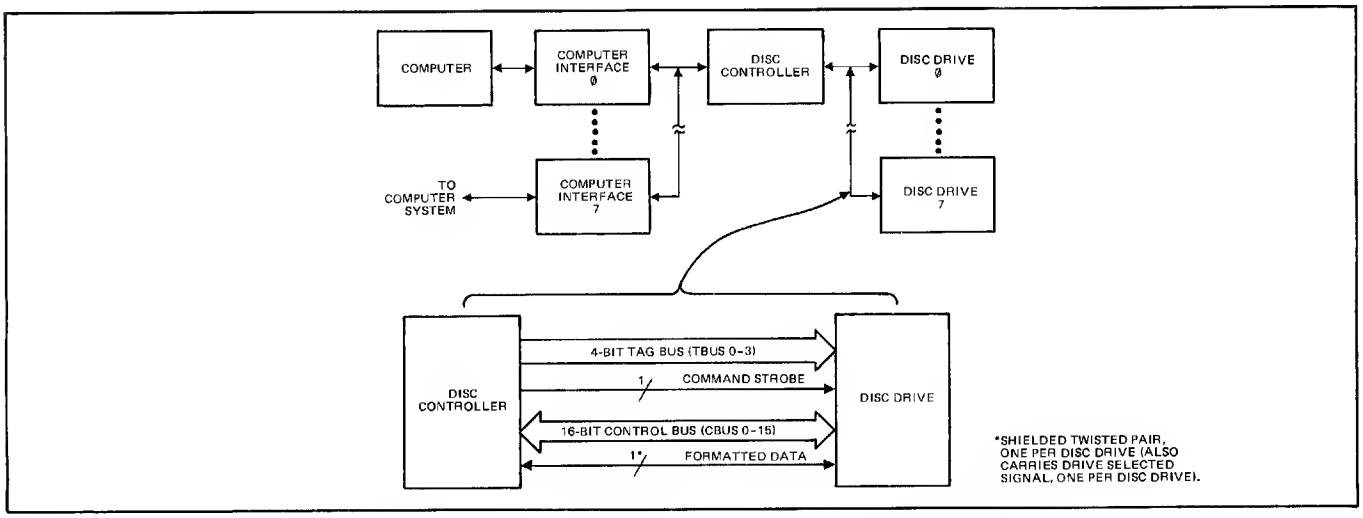

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Figure 4-7. Controller/Disc Drive Interface Block Diagram

Table 4-3. Tag Bus Functions Summary

TAG BUS		CONTROL BUS (Refer to Table 4-4)	
OCTAL CODE	OPERATION		
00	READ*	STATUS	INFORMATION FROM THE DISC DRIVE
01	WRITE*	STATUS	
02	REQUEST STATUS*	STATUS	
03	REQUEST ATTENTION	ATTENTION	
04	DISCONNECT		
05	CLEAR		
06	REQUEST SECTOR*	HEAD-SECTOR ADDRESS	
07			
10	SEEK*	CYLINDER ADDRESS	INFORMATION FROM THE CONTROLLER
11	ADDRESS RECORD*	HEAD-SECTOR ADDRESS	
12	ADDRESS UNIT	UNIT ADDRESS	
13	RECALIBRATE*		
14	TRANSMIT SECTOR*	SECTOR ADDRESS	
15	OFFSET*	OFFSET	
16	CLEAR STATUS*	SELECT CLEAR	
17			

*Only selected units will respond.
Tag bus 3 determines whether controller or disc drive will place information on control bus.
Units respond to commands only after being selected except for Address Unit, Request Attention, Disconnect, and Clear.

Table 4-4. Control Bus Functions Summary

BUS LINE	CLEAR STATUS	OFFSET	CYLINDER	HEAD – SECTOR	UNIT	STATUS	ATTENTION (UNIT)
0	Attention	1	1	Sector 1	1	Drive Busy	0
1	First Status	2	2	2	2	Drive Ready	1
2		4	4	4	4	Seek Check	2
3		8	8	8		First Status	3
4		16	16	16		Drive Fault	4
5		32	32	32		Format	5
6		~~64~~	64			Protected	6
7		Sign	128			Attention	7
8			256	Head 1		Sector Compare	
9			512	2		Drive Type 1	
10				4		Drive Type 2	
11				8		Drive Type 4	
12						Drive Type 8	
13							
14							
15							

4-58. TAG BUS FUNCTIONS. The tag bus is a four-bit bus, validated by command strobe, which transmits drive functions from the controller. All edge validations are by the leading edge of the strobe. Tag bus functions are discussed in detail in table 4-5.

4-59. CONTROL BUS FUNCTIONS. The control bus is a sixteen-bit bidirectional bus used to transmit control information and modifiers between the disc drive and the controller. Depending on the tag bus, the control bus contains one of the functions described in table 4-6.

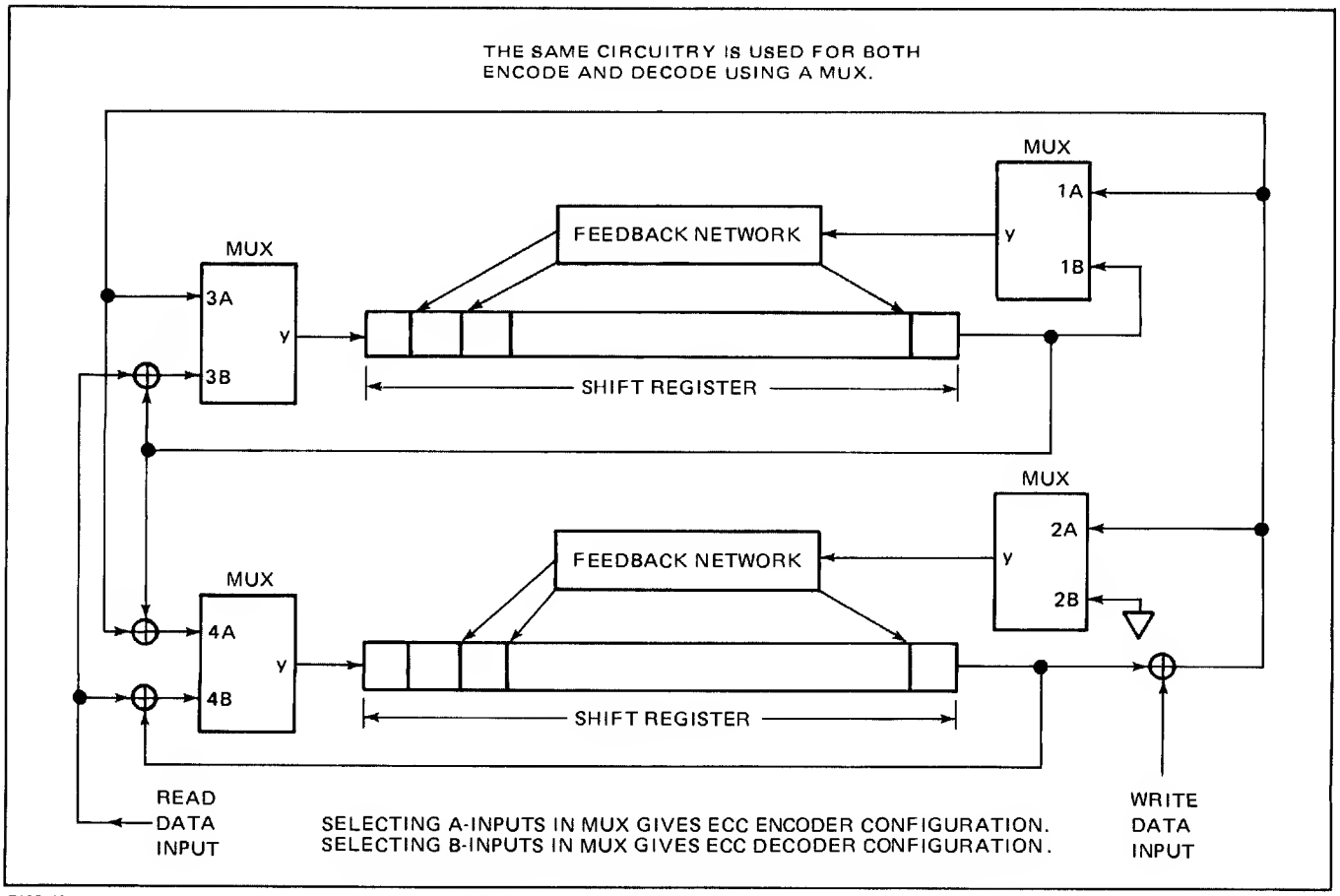
4-60. ERROR CORRECT PCA

4-61. The error eorrect PCA consists of three major functional parts corresponding to the three major functions that are performed on the disc drive subsystem. These functions are write, read and, if required, detect and correct errors by generating an Error Correction Code (ECC). Figure 4-8 is a functional block diagram of the PCA which shows conceptually how the shift registers are switched to perform the various operations.

4-62. ECC ENCODE IMPLEMENTATION. For write operations, serial binary data is supplied to the ECC generator along with the data clock. The A inputs of the multiplexers (MUX) are selected to provide the encoder configuration as shown in figures 4-8 and 4-9. The data entered in the write mode is premultiplied before being divided by the generator polynomial. The shift register is operated in a parallel load mode to facilitate the division process. A control signal is provided to signify the entry of the last data bit. At the end of the data, the check polynomial is retrieved from the ECC generator. This becomes the ECC word to be written in the last word field of a sector on the disc. Control circuitry enables the shift registers to shift out the computed ECC check-polynomial as a bit stream to the disc.

4-63. ECC DECODE IMPLEMENTATION. During read operations, the B inputs of the multiplexers (see figures 4-8 and 4-10) are selected to provide the decoder configuration. Serial data, along with the previously computed check bits, is simultaneously supplied to both read inputs. The input data is also accompanied by the data clock. The received polynomial is reduced by the generator polynomial and a control signal inhibits the shift registers from further computation when the last check bit has been input.

4-64. ECC DETECTION AND CORRECTION. After the last check bit has been read in, the residues in



7103-48

Figure 4-8. Error Correct PCA Functional Block Diagram

Table 4-5. Tag Bus Functions

Read — Select required.
Disc drive gates status on control bus. When this function is true, disc drive waits for leading edge of its internal sector compare signal, transmits sector compare in status word, and transmits bit-encoded data on formatted data lines to the controller.

Write — Select required.
Disc drive gates status on control bus. When this function is true, disc drive waits for leading edge of its internal sector compare signal, transmits sector compare in status word, and accepts bit-encoded data on formatted data lines from the controller.

Request Status — Select required.
When this function is true, disc drive gates contents of its status register on control bus.

Request Attention — Select not required.
When this function is true, disc drive gates its attention bit on control bus line corresponding to its unit number.

Disconnect — Select not required.
Disc drive responds to this function by clearing its select bit. When this bit is false, disc drive will not respond to select-required functions.

Clear — Select not required.
Disc drive clears its attention bit, non-destructive read/write faults, and any other appropriate bits (e.g., first status, sector address register).

Request Sector — Select required.
Disc drive transmits contents of its "current address" counter and head address register on control bus.

Seek — Select required.
Control bus contains cylinder address. On leading edge of command strobe, disc drive clocks control bus contents into its cylinder-address register and initiates a seek to that address. Upon completion of seek, the attention bit is set true. If address is illegal, the disc drive sets seek-check and attention bits; no positioner motion occurs.

Address Record — Select required.
Control bus contains head-sector address. On leading edge of the address record command strobe, the disc drive clocks the control bus contents into its head-sector address register. If address is illegal, it sets the seek-check bit.

Address Unit — Select not required.
Control bus contains a 3-bit unit number. Disc drive responds by setting its select bit if control bus contents match disc-drive address. If this bit is true, it responds to all select-required commands.

Recalibrate — Select required.
Disc drive positions its heads over cylinder 0 and clears its "current-cylinder address" register.

Transmit Sector — Select required.
Control bus contains sector address. On leading edge of command strobe, disc drive clocks sector address only into its sector-address register. Head-address register is not modified.

Offset — Select required.
On leading edge of command strobe, disc drive clocks control-bus contents into its position offset register.

Clear Status — Select required.
Control bus contains bits specifying what disc drive status to clear. Disc drive clears appropriate status bits in response to this function.

Table 4-6. Control Bus Functions

Attention	A line-per-drive response. Each disc drive sets its attention bit when it loads, unloads, completes a seek, or faults. The attention bit is cleared by a clear command or a clear status command with bit 0 *on*. When attention is put on the control bus, each disc drive unit drives only the bus line corresponding to its logical unit number.
Unit	Valid unit numbers are 0 through 7.
Cylinder	Valid cylinder address for the disc drive selected.
Head-sector	Valid head and sector address.
Offset	Valid offset numbers are 0 through 63, positive or negative.
Clear Status	Bit 0 *on* specifies that attention bit should be cleared. Bit 1 *on* specifies that first status bit be cleared.
Status	Contains current disc drive status: Drive Busy — True if heads are not positioned and settled over a valid track. Drive Ready — True if heads are over disc (loaded). Seek Check — Set if controller transmits an invalid cylinder, head, sector address, or if a seek is attempted while disc drive is still executing a previous seek command. Cleared when a valid operation is performed to correct error. Attention bit can then be reset by controller. Note: The bounds checking is done by disc drive. First Status — Set when disc drive first loads heads on disc, i.e., by going from a "not ready" to a "ready" condition. Cleared by a clear status command with bit 1 set. Drive Fault — Set when disc drive detects either a read/write or servo fault; neither can be caused by controller under normal circumstances. Nondestructive read/write faults can be cleared by a clear command. Servo faults and destructive read/write faults unload heads, and therefore require operator intervention. Format — Transmits condition of FORMAT switch located at front of disc drive. This switch may be set to up (or •) position to allow track initialization. Protected — Transmits condition of platter protect (read only) switch located on front of disc drive. Attention — Condition of attention bit. Cleared by a clear status command with bit 0 set. Sector Compare — True while a read or write command is true following coincidence of a leading edge of disc drive's internal signal comparing sector address register and "current sector address" counter. Cleared when command is removed or when disc drive determines that it is not safe to continue transfer because sector has almost passed.
Drive Type	Four encoded bits which allows controller to determine number of heads and number of sectors per track.
Command Strobe Line	Validates all functions on tag bus. A function is valid only if this line is true. If an edge is used it must be leading edge.
Formatted Data Lines	A differential pair used to transmit serial bit formatted data to and from disc drive.

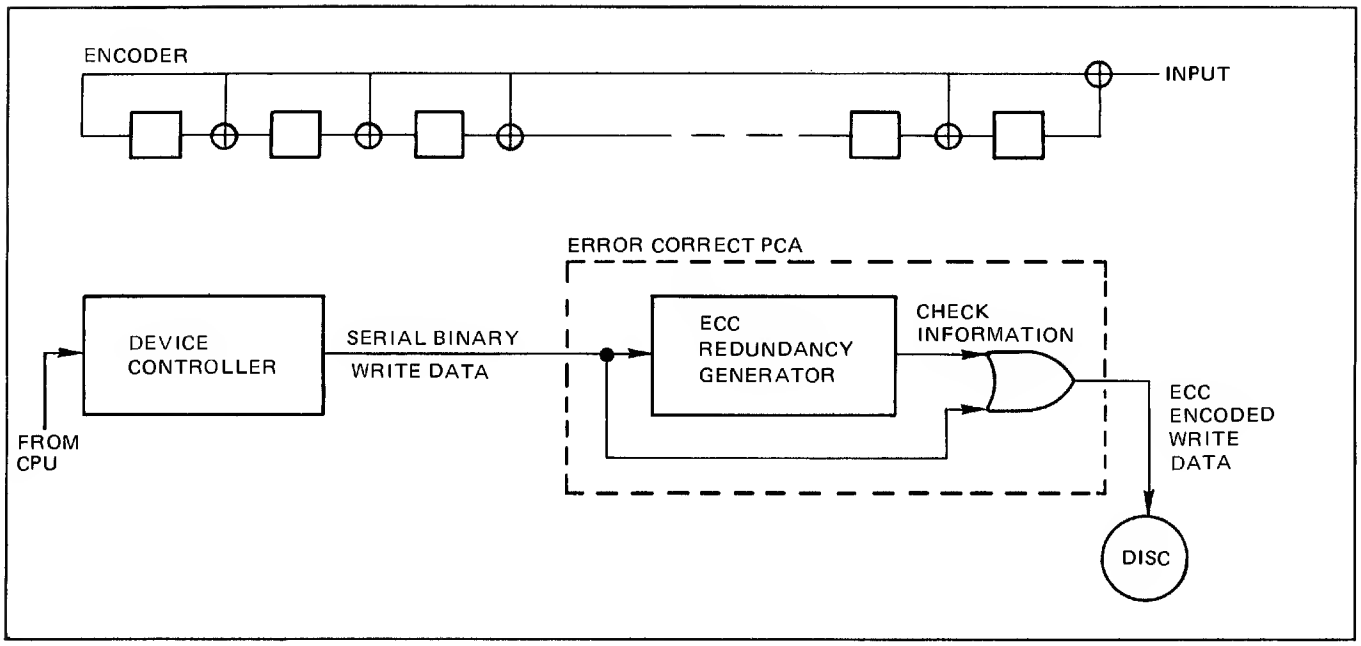


Figure 4-9. ECC Write Circuit

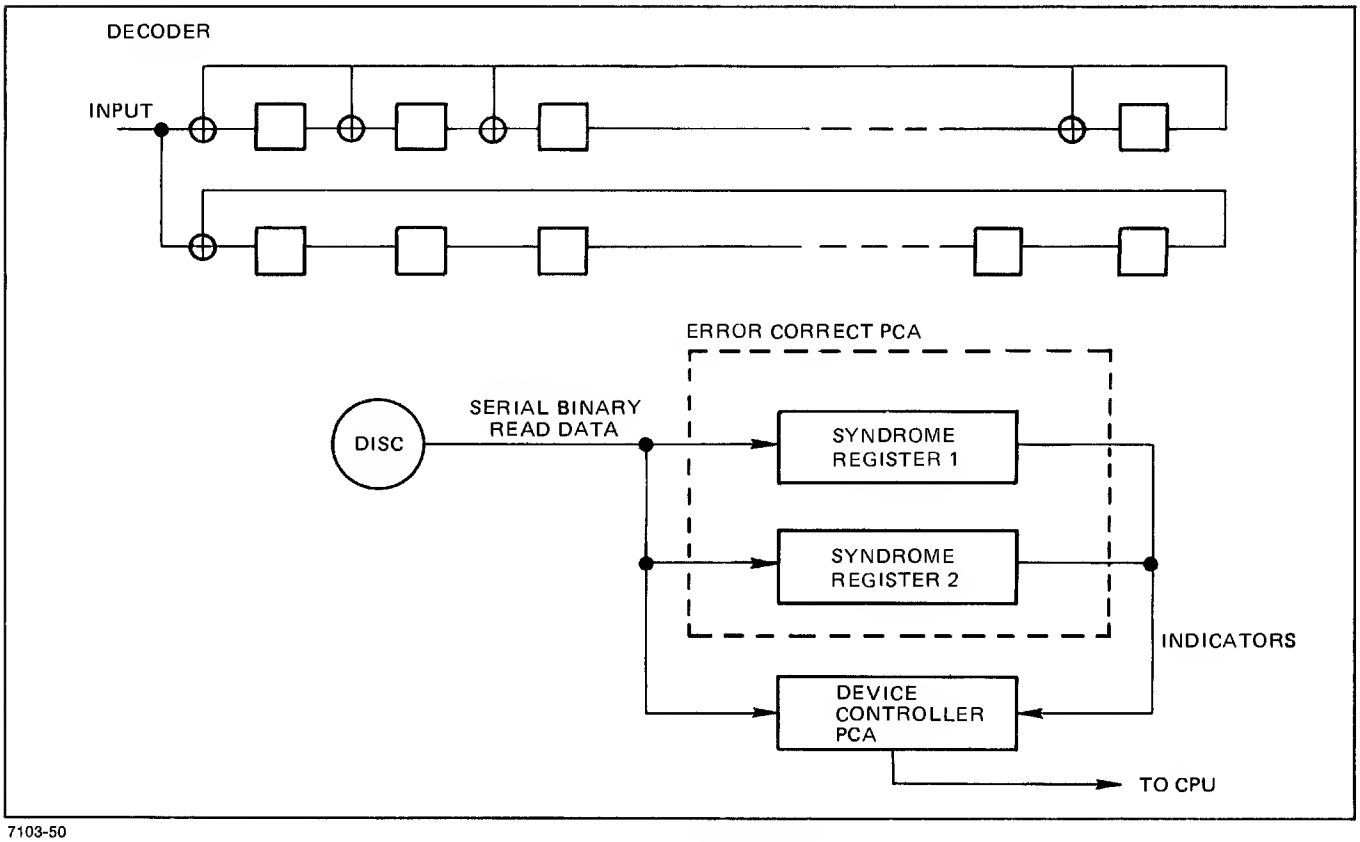


Figure 4-10. ECC Read Circuit

the registers are checked for values not equalling 0 by the check-for-0-syndrome circuitry which consists of a network of "or" gates. The device controller checks the two syndrome indicators and decides if an error has occurred. For detection of errors, the ECC detector identifies the following types:

a. If both syndromes are 0, there is no error.

b. If only one syndrome is 0, an uncorrectable error has occurred.

c. If both syndromes are not 0, a possibly correctable error has occurred.

4-65. The device controller PCA then interrupts the CPU interface and reports the appropriate status that describes one of the above conditions and awaits the next command. If a possibly correctable error was reported to the CPU interface and the device controller PCA subsequently receives the REQUEST SYNDROME command from the computer, the error correction algorithmn stored in ROM of the microprocessor PCA is invoked. Execution of the algorithm is accomplished by the ALU in the microprocessor. This algorithm terminates with either of two possible outcomes: the error is uncorrectable, or the error is correctable and the information required to correct the error has been successfully computed. If the error is correctable, the data pattern can be obtained by shifting the syndromes in their respective registers until they have the same representations. The error pattern required to correct the error is then sent to the computer. For further detail of the REQUEST SYNDROME command, refer to the description in section III.

4-66. POWER SUPPLY

4-67. The controller power supply (see figure 4-11) consists of a printed circuit assembly (PCA) and various electronic components mounted in the rear portion of the controller chassis. The dc power is supplied to the controller PCA's through each board's power connector P1. The power supply provides +5V @ 20A, -5V @ 300 mA, -20V (unregulated), and a power up signal to the controller logic. Overvoltage and overcurrent protection circuits and fuses in the transformer primary and secondary circuits protect the controller logic boards.

4-68. The input line voltage is reduced to the proper level by the power transformer and is coupled to the rectifier and filter. Series-pass transistors act as variable resistances to keep the output voltage constant. The series-pass transistors are driven by an error amplifier and comparator which compares the output voltage to a reference voltage. Current sense circuitry detects an overcurrent condition and shuts down the series-pass transistors by grounding the output of the error amplifier. If an overvoltage condition is detected, the power supply is shut down. The -5 volt supply is rectified, filtered, and regulated independently from the +5 volt supply. The unregulated -15 volt supply is generated with a voltage doubler.

4-69. The power supply will operate on nominal line voltages of 100V, 120V, 220V, and 240V. Line voltage selection is accomplished by configuring jumpers on the transformer. (See figure 2-3.) The line filter accepts the line cord, directs the line current through a fuse, and selects the proper power-transformer primary wires in such a way that the fans always receive a nominal 120 VAC regardless of the line voltage. The power supply will operate on 50 Hz or 60 Hz with no adjustments. The filter capacitor and power transformer are bolted to the rear of the chassis behind the power regulator board.

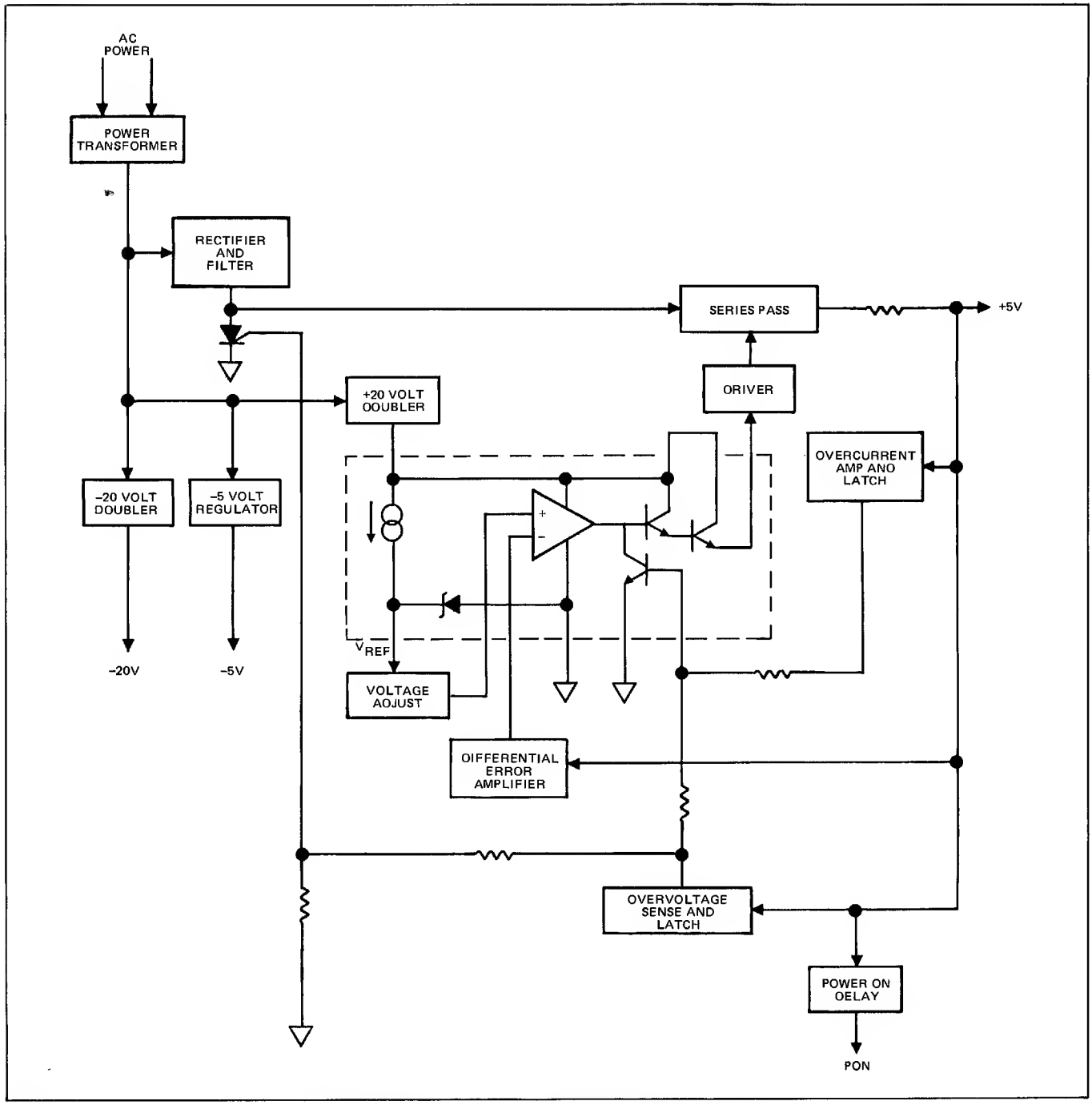
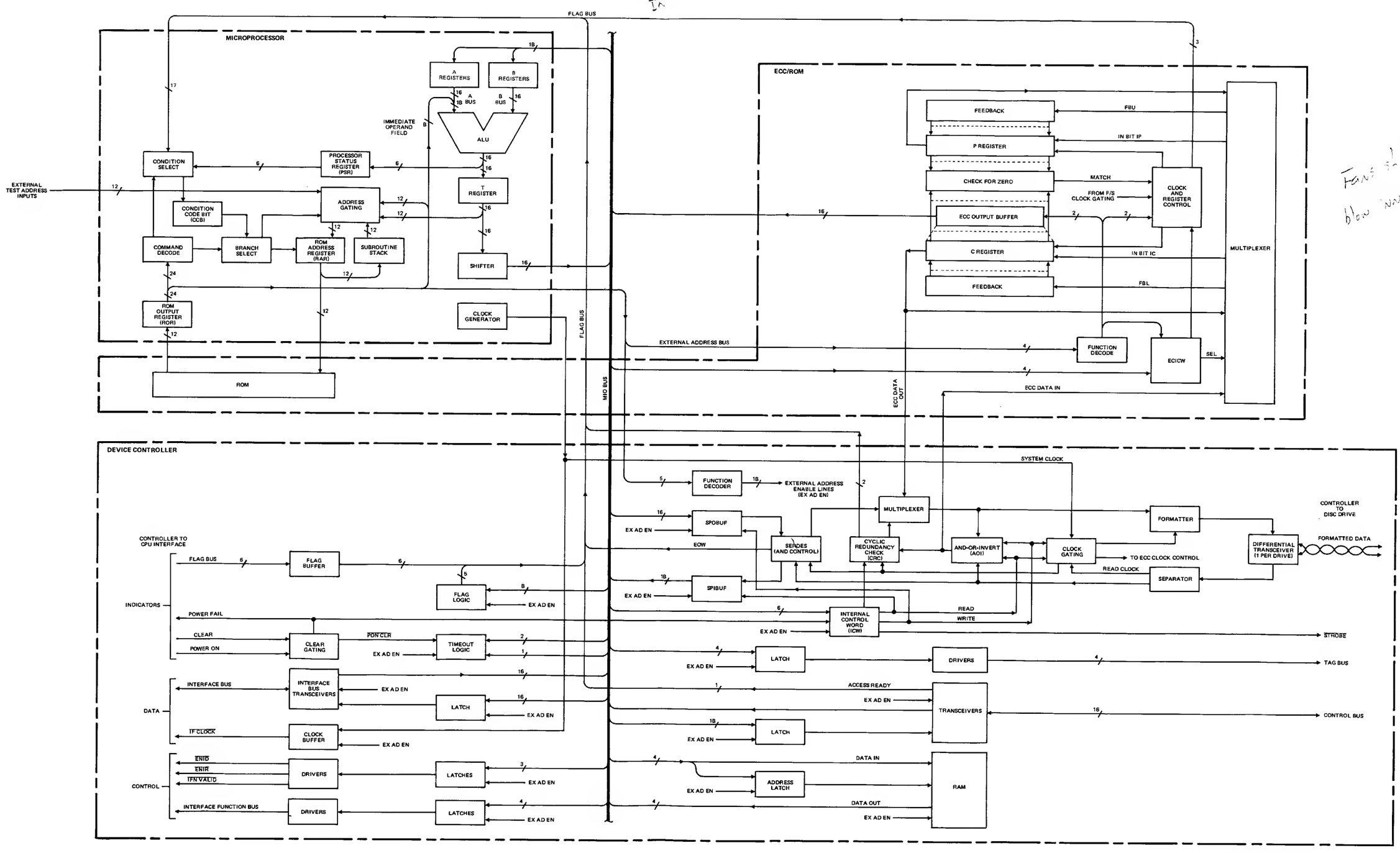


Figure 4-11. Power Supply Functional Block Diagram



REF 7103-61

Figure 4-12. Controller Detailed Functional Block Diagram

SERVICE

SECTION V

5-1. INTRODUCTION

5-2. This section includes general servicing information, maintenance reference material, preventive maintenance, and troubleshooting.

5-3. GENERAL SERVICING INFORMATION

5-4. Ensure that controller printed-circuit assemblies (PCA's) remain firmly installed in their PCA module slots with the extractor handles locked in place. All cables should also be firmly attached to connectors.

5-5. Dangerous voltages are present in the controller. Use caution when working on controller components. It is essential that all cautions and warnings stated in cabinet or other maintenance documents be observed.

WARNING

Hazardous voltages are exposed when the top cover is removed.

5-6. Before removing or installing controller PCA's, set the POWER switch to OFF to remove power from the PCA connectors. Also follow this procedure for PCA extender assemblies.

5-7. POWER DISTRIBUTION

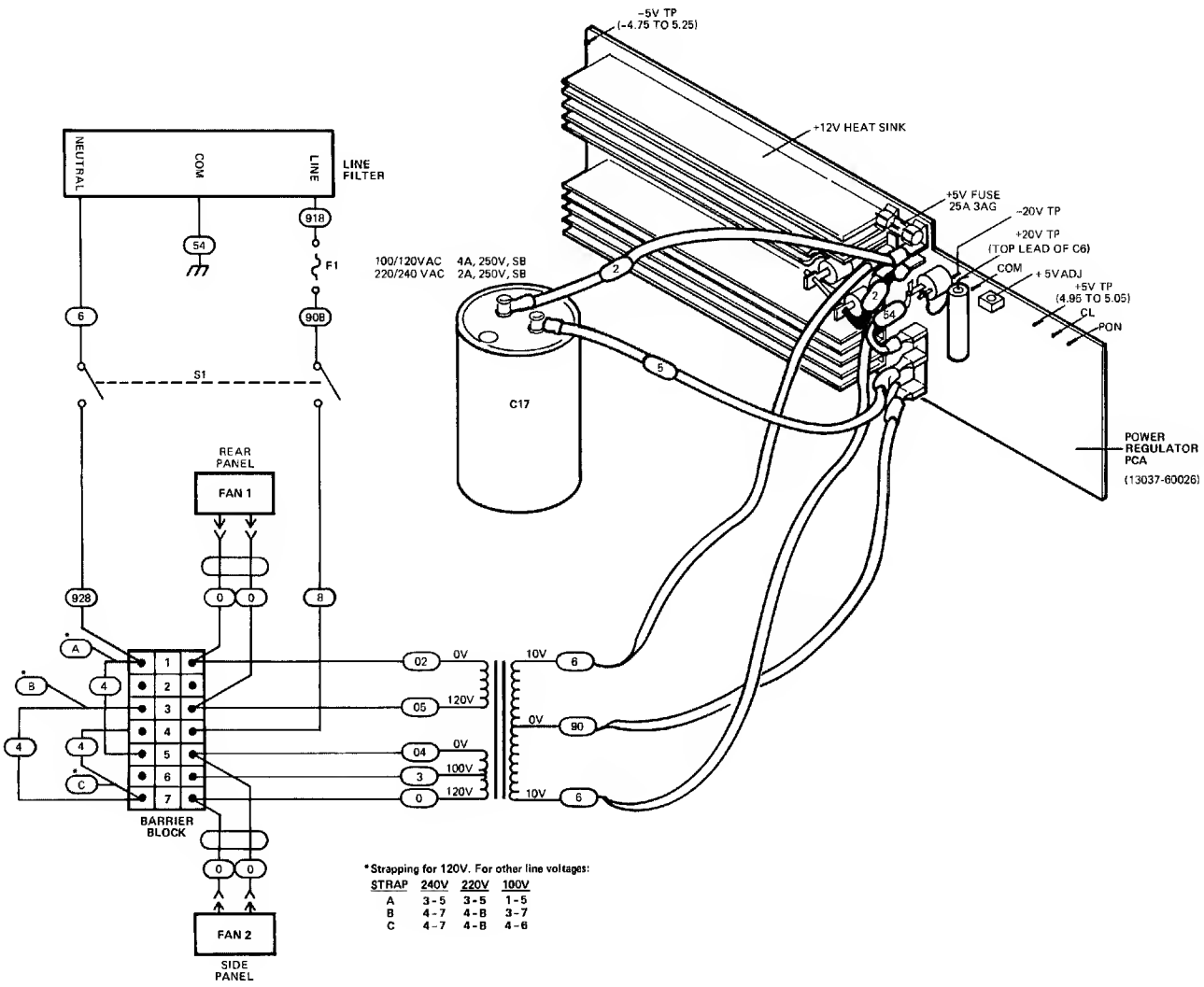
5-8. Power distribution for the controller is shown in figure 5-1. This diagram applies only when the three PCA's are enclosed in the controller chassis. If the controller chassis is not used where the PCA's are installed separately in a system configuration, refer to the appropriate documentation for that system.

5-9. PREVENTIVE MAINTENANCE

5-10. There are no extensive procedures required for maintaining the controller. Cleaning and inspection should be done semiannually. The 5-volt power supplies should be monitored at the same time to ensure that the output voltages are within the accepted tolerances and both fans should be checked to ensure that they start during power application.

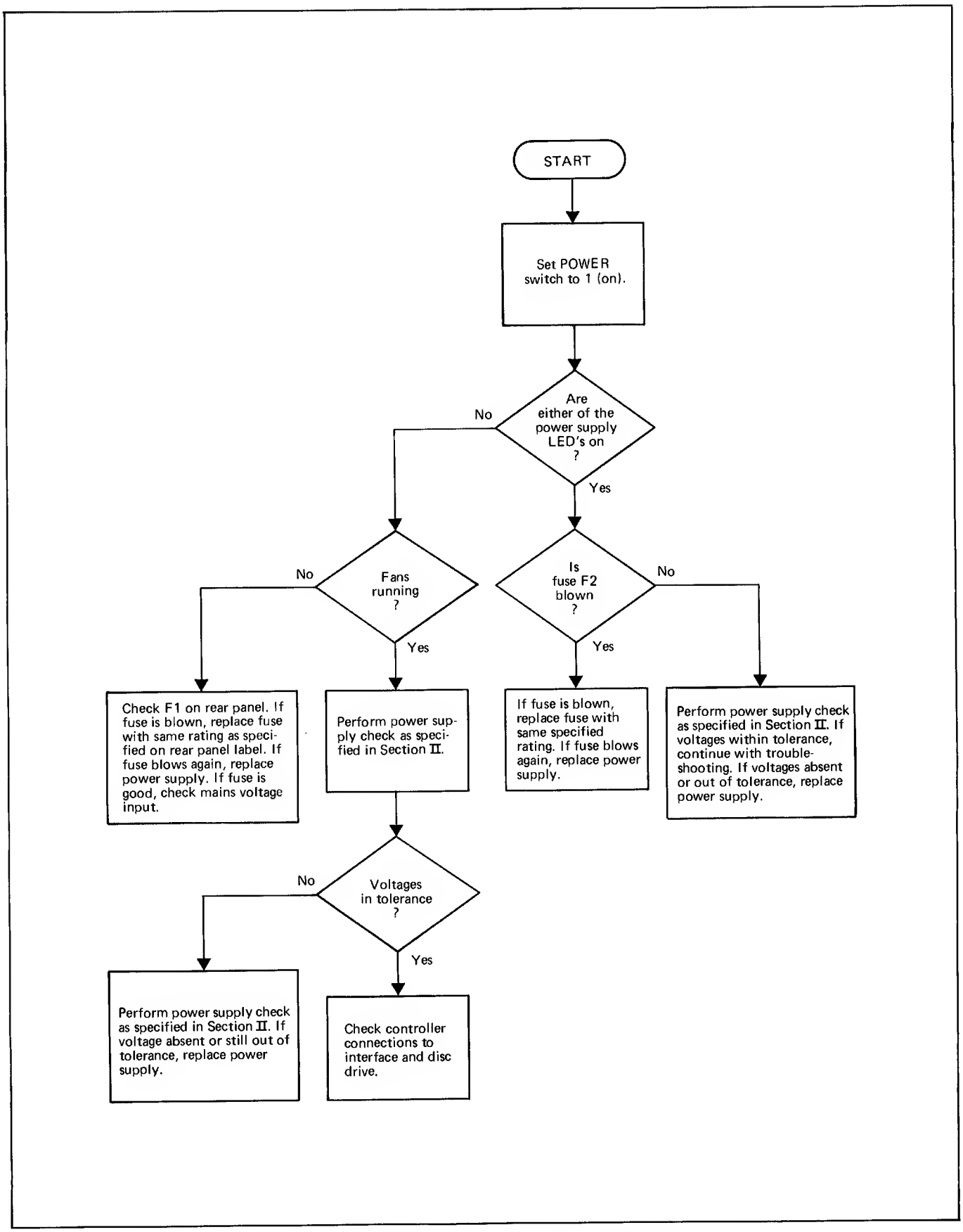
5-11. TROUBLESHOOTING

5-12. The troubleshooting philosophy for the controller is to check the power input, power supplies for the PCA's, make a visual inspection of all cables and connectors, and change one of the four PCA's if the problem is not found in one of the previous areas. An appropriate diagnostic can be run if the controller is connected to an HP computer system. Refer to the applicable subsystem manual for operation and interpretation of the diagnostic. Figure 5-2 is a troubleshooting flowchart which presents a sequential procedure for checking power input and the PCA power supplies.



7103-62

Figure 5-1. Controller Power Distribution



7103-6A

Figure 5-2. Power Supply Troubleshooting Flowchart

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This section provides listings of all field-replaceable parts and an illustrated parts breakdown for the 13037C Controller, as well as replaceable part ordering information.

Replaceable parts for the controller are listed in disassembly order in table 6-1 and illustrated in figure 6-1. In the replaceable parts listing, attaching parts are listed immediately after the item they attach. Items in the DESCRIPTION column are indented to indicate their relationship. In addition, the symbol "— — — x — — —" follows the last attaching part for that item. Indentation is as follows:

MAJOR ASSEMBLY
*Replaceable Assembly
*Attaching Parts for Replaceable Assembly
**Subassembly or Component Part
**Attaching Parts for Subassembly or Component Part

The replaceable parts listings provide the following information for each part:

a. FIG. & INDEX NO. The figure and index number which indicates where the replaceable part is illustrated.

b. HP PART NO. The Hewlett-Packard part number for each replaceable part.

c. DESCRIPTION. The description of each replaceable part. Refer to table 6-2 for an explanation of those abbreviations used in the DESCRIPTION column.

d. MFR CODE. The five-digit code that denotes a typical manufacturer of a part. Refer to table 6-3 for a listing of manufacturers that correspond to the codes.

e. MFR PART NO. The manufacturer's part number of each replaceable part.

f. UNITS PER ASSEMBLY. The total quantity of each part used in the major assembly.

The MFR CODE and MFR PART NO. for common hardware items are listed as 00000 and OBD (order by description), respectively, because these items can usually be purchased locally.

Component parts of printed-circuit assemblies (PCA's) are not included since these parts are considered replaceable only at the factory or a depot. An individual PCA can be ordered by the following part number:

Microprocessor	13037-60001
Device Controller	13037-60028
ECC/ROM	13037-60024
Power Regulator	13037-60026

6-2. ORDERING INFORMATION

To order replaceable parts for the controller, address the order to your local Hewlett-Packard Sales and Support Office. Sales and Support Offices are listed at the back of this manual. Specify the following information for each part ordered:

a. Model and full serial number.

b. Hewlett-Packard part number.

c. Complete description for each part as provided in the replaceable parts listings.

Table 6-1. HP 13037D Disc Controller, Replaceable Parts

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-	13037D	DISC CONTROLLER	28480	13037D	
1	13037-60052	*FRONT PANEL	28480	13037-60052	1
2	1390-0473	**FASTENER, captive screw retainer, 0.161 in. ID	94222	09-49-101-12	4
3	1390-0484	**FASTENER, captive screw, 0.19 in. dia	94222	09-99-123-26	4
4	7120-1254	**HP LOGO	28480	7120-1254	1
5	2200-0140	**SCREW, fh, pozi, 4-40, 0.25 in. long	00000	OBD	16
6	13037-00038	**CLAMP	28480	13037-00038	8
7	8160-0447	**RFI FINGER	28480	8160-0447	8
8	0400-0018	*GROMMET, notched, 0.052 in. groove width, 10.0 in. long	03296	G-51H-A	1
9	13037-00016	*DATA CABLE CLAMP BRACKET	28480	13037-00016	1
10	13037-60028	*DEVICE CONTROLLER PCA	28480	13037-60028	1
11	13037-60021	*JUMPER CABLE ASSEMBLY	28480	13037-60021	1
12	13037-60001	*MICROPROCESSOR PCA	28480	13037-60001	1
13	13037-60024	*ERROR CORRECT (ECC/ROM) PCA	28480	13037-60024	1
14	13037-00034	*BRACKET, data cable	28480	13037-00034	1
15	13037-00033	*BRACKET, main cable	28480	13037-00033	1
16	8120-1378	*POWER CORD, NEMA5/CEE	28480	8120-1378	1
	8120-1351	*POWER CORD, BS1363/CEE	28480	8120-1351	REF
	8120-1369	*POWER CORD, ASC112/CEE	28480	8120-1369	REF
	8120-1689	*POWER CORD, GMBH/CEE	28480	8120-1689	REF
	8120-1860	*POWER CORD, CEE/CEE	28480	8120-1860	REF
	8120-2104	*POWER CORD, SEV/CEE	28480	8120-2104	REF
	8120-2956	*POWER CORD, MDPP/CEE	28480	8120-2956	REF
17	13037-00028	*COVER, top/bottom	28480	13037-00028	2
		(Attaching Parts)			
18	2200-0140	*SCREW, fh, pozi, 4-40, 0.25 in. long	00000	OBD	6
19	2360-0119	*SCREW, ph, pozi, 6-32, 0.437 in. long	00000	OBD	3
20	3050-0407	*WASHER, flat, no. 6, 0.164 in. thick	00000	OBD	3
		- - - X - - -			
21	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	2
22	3050-0228	*WASHER, flat, no. 6, 0.156 in. thick	00000	OBD	2
23	13037-00027	*COVER, side	28480	13037-00027	2
24	13037-00018	*SHIELD, AC power	28480	13037-00018	1
		(Attaching Parts)			
25	2360-0119	*SCREW, ph, pozi, 6-32, 0.437 in. long	00000	OBD	2
26	3050-0228	*WASHER, flat, no. 6, 0.156 in. thick	00000	OBD	2
		- - - X - - -			
27	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	1
28	2510-0100	*SCREW, fh, 100-deg, 8-32, 0.312 in. long	00000	OBD	8
29	13037-00032	*SHIELD, power supply	28480	13037-00032	1
		(Attaching Parts)			
30	2360-0115	*SCREW, ph, pozi, 6-32, 0.312 in. long	00000	OBD	4
		- - - X - - -			
31	13037-20013	*FRAME CASTING, rear, 5.25 in. high	28480	13037-20013	1
32	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	4
33	2360-0125	*SCREW, ph, pozi, 6-32, 0.75 in. long	00000	OBD	4
34	2420-0001	*NUT, hex, 6-32, w/ext-tooth	00000	OBD	4
35	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	4

Table 6-1. HP 13037D Disc Controller, Replaceable Parts (Continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
36	2190-0464	*WASHER, flat, no. 6, 0.156 in. ID	00000	OBD	4
37	3160-0099	*FAN GRILLE	23936	5504	1
38	2420-0001	*NUT, hex, 6-32, w/ext-tooth	00000	OBD	4
39	3160-0341	*FAN, tubeaxial, 115-CFM, 115V, 50/60 Hz	28875	BS-2107F-510H	1
40	2680-0271	*SCREW, ph, pozi, 10-32, 0.312 in. long	00000	OBD	2
41	2360-0117	*SCREW, ph, pozi, 6-32, 0.312 in. long	00000	OBD	3
42	3050-0407	*WASHER, flat, no. 6, 0.164 in. ID	00000	OBD	3
43	2420-0001	*NUT, hex, 6-32, w/ext-tooth	00000	OBD	2
44	0363-0166	*RFI FINGER	28480	0363-0166	2
45	2580-0003	*NUT, hex, w/lock washer, 8-32, 0.125 in. thick	00000	OBD	1
46	2510-0109	*SCREW, ph, pozi, 8-32, 0.625 in. long	00000	OBD	1
47	0180-1958	*CLAMP, capacitor, 3 in. dia., stl	56289	4586-2-DZZ	1
48	0180-2789	*CAPACITOR, fixed, 0.076F, +75 -10% 15 Vdc, A1	56289	602D911-DHX	1
49	3101-2377	*SWITCH, rocker, subminiature, dpdt, 5A, 250 Vac, spade lug	09353	9221J3Z4Q	1
		(Attaching Parts)			
50	2260-0009	*NUT, hex, w/lock washer, 4-40, 0.094 in. thick	00000	OBD	2
51	0380-0174	*STANDOFF, 4-40, 0.25 in. long	06540	8077-B-0440-28	2
		- - - X - - -			
52	2110-0565	*CAP, fuseholder, 12A maximum for UL	28480	2110-0565	1
53	2110-0365	*FUSE, 4A, 250V	71400	MDA-4A	1
	2110-0303	*FUSE, 2A, 250V	71400	MDX-2A	REF
54	2110-0569	*NUT, fuseholder, M12.7 by 1.5 dbl	28480	2110-0569	1
55	2110-0566	*BODY, fuseholder, 12A, 250V	28480	2110-0566	1
56	2420-0001	*NUT, hex, 6-32, w/ext-tooth	00000	OBD	1
57	2190-0468	*WASHER, spring, slotted, no. 10, 0.207 in. ID	00000	OBD	1
58	9135-0106	*FILTER, line, CEE type 22 terminals	23880	F14282	1
		(Attaching Parts)			
59	2200-0107	*SCREW, ph, pozi, 4-40, 0.375 in. long	00000	OBD	2
60	3050-0229	*WASHER, flat, no. 4, 0.125 in. ID	00000	OBD	2
		- - - X - - -			
61	2580-0003	*NUT, hex, w/lock washer, 8-32, 0.125 in. thick	00000	OBD	2
62	2510-0111	*SCREW, ph, pozi, 8-32, 0.75 in. long	00000	OBD	2
63	0360-1918	*BARRIER BLOCK, 7-terminal, twin screw phenolic	71785	354-61-07-001	1
64	0360-0625	*MARKER STRIP, w/numerals 1 through 7	75382	MS-671-7-1A	1
65	9100-0438	*POWER TRANSFORMER	28480	9100-0438	1
		(Attaching Parts)			
66	2680-0051	*SCREW, ph, pozi, 10-32, 0.375 in. long	00000	OBD	4
67	2190-0402	*WASHER, flat, no. 10, 0.203 in. ID	00000	OBD	4
		- - - X - - -			

Table 6-1. HP 13037D Disc Controller, Replaceable Parts (Continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
68	13037-00022	*PLATE, power, 100/120 Volt	28480	13037-00022	1
	13037-00023	*PLATE, power, 220/240 Volt (OPT 015)	28480	13037-00023	REF
		(Attaching Parts)			
69	2200-0105	*SCREW, ph, pozi, 4-40, 0.312 in. long	00000	OBD	2
70	3050-0229	*WASHER, flat, no. 4, 0.125 in. ID	00000	OBD	2
		- - - X - - -			
71	13037-00035	*CHASSIS, power module	28480	13037-00035	1
72	13037-60026	*POWER REGULATOR PCA	28480	13037-60026	1
		(Attaching Parts)			
73	2510-0101	*SCREW, ph, pozi, 8-32, 0.312 in. long	00000	OBD	2
74	2190-0073	*WASHER, lock, hlcl, no. 8, 0.168 in. ID	00000	OBD	2
75	2360-0195	*SCREW, ph, pozi, 6-32, 0.312 in. long	00000	OBD	4
76	2190-0006	*WASHER, lock, hlcl, no. 6, 0.141 in. ID	00000	OBD	4
		- - - X - - -			
77	13037-60022	*INTERCONNECTING CABLE, 3 connector	28480	13037-60022	2
		(Attaching Parts)			
78	2200-0111	*SCREW, ph, pozi, 4-40, 0.5 in. long	00000	OBD	6
79	3050-0229	*WASHER, flat, no. 4, 0.125 in. ID	00000	OBD	6
		- - - X - - -			
80	13037-60027	*POWER INTERCONNECT PCA	28480	13037-60027	1
		(Attaching Parts)			
81	2200-0105	*SCREW, ph, pozi, 4-40, 0.312 in. long	00000	OBD	10
		- - - X - - -			
82	13037-20003	*GUIDE, PC board, rear	28480	13037-20003	2
		(Attaching Parts)			
	2360-0125	*SCREW, ph, pozi, 6-32, 0.75 in. long	00000	OBD	2
	3050-0228	*WASHER, flat, no. 6, 0.156 in. ID	00000	OBD	2
		- - - X - - -			
83	0400-0082	*GROMMET, notched, 0.085 in. groove width, 3.5 in. long	03296	G-51H-B	1
84	0400-0082	*GROMMET, notched, 0.085 in. groove width, 0.75 in. long	03296	G-51H-B	1
85	8160-0446	*RFI FOAM STRIP	28480	8160-0446	1
86	13037-00003	*MOUNTING FRAME, power regulator	28480	13037-00003	1
		(Attaching Parts)			
	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	4
	2680-0053	*SCREW, ph, pozi, 10-32, 0.438 in. long	00000	OBD	4
		- - - X - - -			
87	2360-0127	*SCREW, ph, pozi, 6-32, 0.875 in. long	00000	OBD	4
88	3050-0228	*WASHER, flat, no. 6, 0.156 in. ID	00000	OBD	4
89	5000-8015	*FAN GRILLE	28480	5000-8015	1
90	2190-0464	*WASHER, flat, no. 6	00000	OBD	4
91	2420-0001	*NUT, hex, 6-32, w/ext-tooth	00000	OBD	4
92	3160-0341	*FAN, tubeaxial, 115-CFM, 115V, 50/60 Hz	28875	BS-2107F-510H	1
93	0403-0372	*GUIDE, PC board, plastic, 10.615 in. long, 0.375 in. thick	28480	0403-0372	1
		(Attaching Parts)			
	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	4
	3050-0228	*WASHER, flat, no. 6, 0.156 in. ID	00000	OBD	4
		- - - X - - -			

Table 6-1. HP 13037D Disc Controller, Replaceable Parts (Continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
94	0400-0082	*GROMMET, notched, 0.085 in. groove width, 1.25 in. long	03296	G-51H-B	1
95	13037-00001	*BRACKET, PC guide	28480	13037-00001	1
		(Attaching Parts)			
	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	2
	2680-0053	*SCREW, ph, pozi, 10-32, 0.438 in. long	00000	OBD	2
	0380-0637	*STANDOFF, square, 6-32, 1.062 in. long	06540	8639-A-0632-16	2
		- - - X - - -			
96	0400-0082	*GROMMET, notched, 0.085 in. groove width, 1.0 in. long	03296	G-51H-B	1
97	13037-00020	*MOUNTING BRACKET, data cable clamp	28480	13037-00020	1
		(Attaching Parts)			
	2680-0053	*SCREW, ph, pozi, 10-32, 0.438 in. long	00000	OBD	2
		- - - X - - -			
98	0400-0082	*GROMMET, notched, 0.085 in. groove width, 1.25 in. long	03296	G-51H-B	1
99	13037-00001	*BRACKET, PC guide	28480	13037-00001	1
		(Attaching Parts)			
	2360-0017	*SCREW, rdh, st1, 6-32, 1.375 in. long	00000	OBD	2
		- - - X - - -			
100	1400-0440	*CABLE TIE, 0.062 in. long, 0.75 in. dia, 0.184 in. wide nylon	06383	PLC2S-S10-M	2
		(Attaching Parts)			
101	2420-0001	*NUT, hex, w/lock washer, 6-32, 0.109 in. thick	00000	OBD	1
102	3050-0228	*WASHER, flat, no. 6, 0.156 in. ID	00000	OBD	1
103	2360-0201	*SCREW, ph, pozi, 6-32, 0.5 in. long	00000	OBD	1
		- - - X - - -			
104	13037-20010	*CORNER STRUT	28480	13037-20010	2
		(Attaching Parts)			
	2510-0100	*SCREW, fh, 100-deg, 8-32, 0.312 in. long	00000	OBD	2
		- - - X - - -			
105	0403-0372	*GUIDE, PC board, plastic, 10.615 in. long, 0.375 in. thick	28480	0403-0372	1
		(Attaching Parts)			
	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	4
	0350-0228	*WASHER, flat, no. 6, 0.156 in. ID	00000	OBD	4
		- - - X - - -			
106	13037-00019	*MOUNTING PLATE, PC guide	28480	13037-00019	1
		(Attaching Parts)			
	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	2
		- - - X - - -			
107	13037-00002	*MOUNTING PLATE, PC guide	28480	13037-00002	1
		(Attaching Parts)			
	2360-0117	*SCREW, ph, pozi, 6-32, 0.375 in. long	00000	OBD	2
		- - - X - - -			
108	13037-20010	*CORNER STRUT	28480	13037-20010	2
		(Attaching Parts)			
	2510-0100	*SCREW, fh, 100-deg, 8-32, 0.312 in. long	00000	OBD	2
		- - - X - - -			

Table 6-1. HP 13037D Disc Controller, Replaceable Parts (Continued)

FIG.& INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
109	13037-00015	*MOUNTING BRACKET, front panel	28480	13037-00015	2
		(Attaching Parts)			
110	2360-0119	*SCREW, ph, pozi, 6-32, 0.437 in. long	00000	OBD	2
111	3050-0228	*WASHER, flat, no. 6, 0.152 in. ID	00000	OBD	2
		- - - X - - -			
112	0363-0166	*RFI FINGER	28480	0363-0166	8
		(Attaching Parts)			
113	2200-0137	*SCREW, ph, pozi, 4-40, 0.188 in. long	00000	OBD	1
		- - - X - - -			
114	13037-60050	*FRONT FRAME CASTING	28480	13037-60050	1

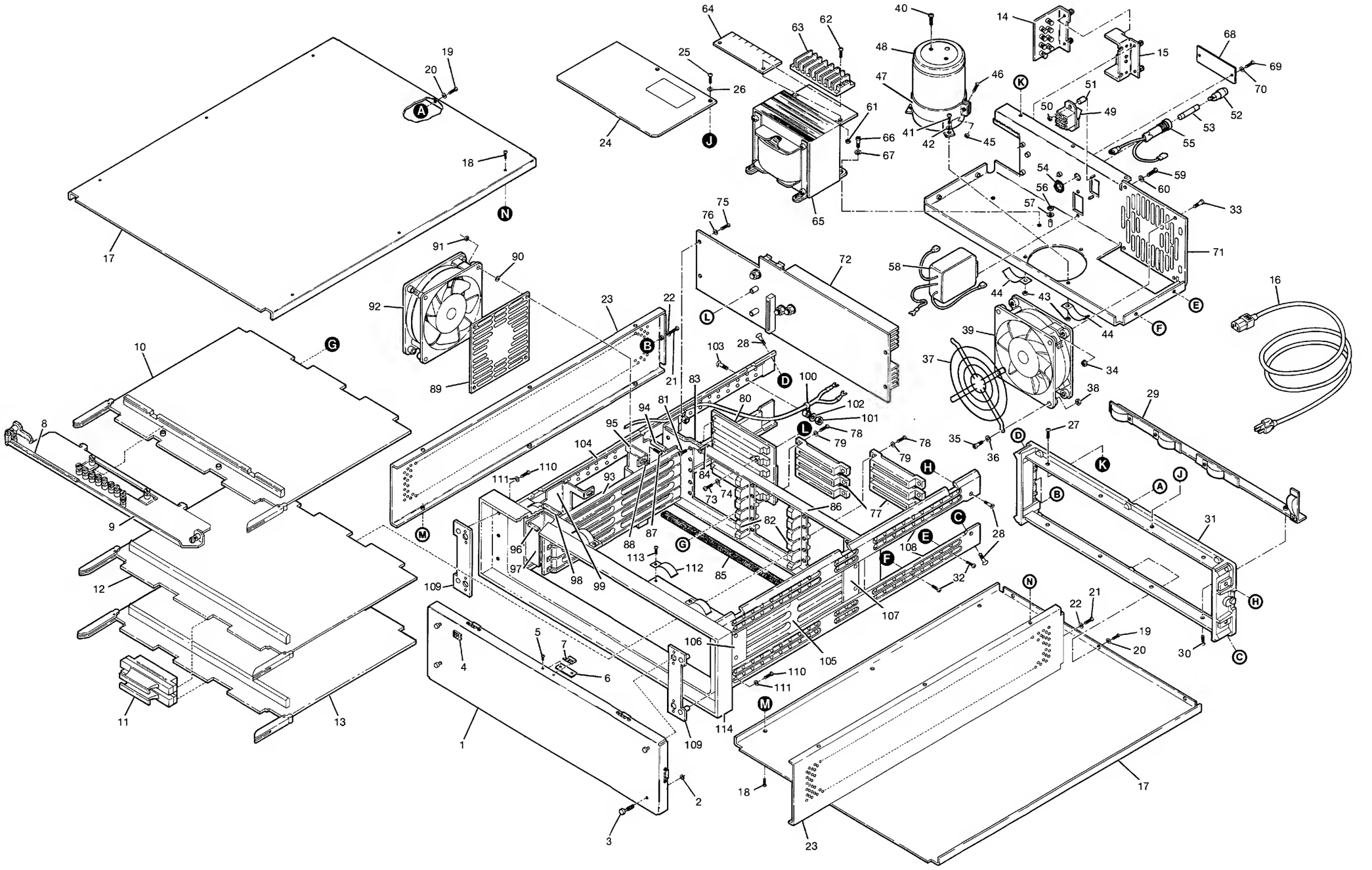


Figure 6-1. HP 13037D Disc Controller, Exploded View

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A = assembly	J = jack, receptacle connector	T = transformer
B = blower, fan, motor, synchro	K = relay	TB = terminal board
C = capacitor	L = inductor	TP = test point
CB = circuit breaker	M = meter	U = integrated circuit, non-repairable assembly
CR = diode	MP = mechanical part	
DS = indicator lamp	P = plug connector	VR = voltage retulator
E = contact, miscellaneous electrical part	Q = semiconductor device other than diode or integrated circuit	W = cable assembly (with connectors), wire
F = fuse	R = resistor	X = socket
FL = filter	RT = thermistor	Y = crystal unit
H = hardware	S = switch	Z = network, tuned circuit

ABBREVIATIONS

A = ampere(s)	ID = inside diameter	qty = quantity
ac = alternating current	in. = inch, inches	
AR = as required	incand = incandescent	rdh = round head
assy = assembly	incl = include(s)	rect = rectifier
	intl = internal	ref = reference
brkt = bracket	I/O = input/output	rf = radio frequency
		rfi = radio frequency interference
c = centi(10^{-2})	k = kilo (10^{3}), kilohm	rh = right hand
C = Celsius, centigrade	kg = kilogram	rpm = revolutions per minute
cer = ceramic		rwv = reverse working voltage
cm = centimetre	lb = pound	
comp = composition	LED = light-emitting diode	sb = slow blow
conn = connector	lh = left hand	SCR = semiconductor-controlled rectifier
	M = mega (10^{6}), megohm	
d = deci(10^{-1})	m = milli (10^{-3})	scw = square cone washer
dc = direct current	mach = machine	Se = selenium
deg = degree(s)	mb = medium blow	Si = silicon
dia = diameter	met oxd = metal oxide	slftpg = self-tapping
dpdt = double-pole, double-throw	mfr = manufacturer	spdt = single-pole, double throw
dpst = double-pole, single-throw	misc = miscellaneous	spst = single-pole, single throw
	mm = millimetre	sst = stainless steel
elctlt = electrolytic	mtg = mounting	stl = steel
encap = encapsulated	My = Mylar	sw = switch
ext = external		
	n = nano (10^{-9})	T = TORX® screw
F = Fahrenheit, farad	n.c. = normally closed	Ta = tantalum
fb = fast blow	no. = number	tgl = toggle
fh = flat head	n.o. = normally open	thd = thread
fig. = figure	NSR = not separately replaceable	Ti = titanium
filh = fillister head	ntd = no time delay	tol = tolerance
flm = film		
fw = full wave	OBD = order by description	U (μ) = micro (10^{-6})
fxd = fixed	OD = outside diameter	
	ovh = oval head	V = volt(s)
G = giga(10^{9})	oxd = oxide	var = variable
Ge = germanium		Vdcw = direct current working volts
	p = pico (10^{-12})	
H = henry, henries	PCA = printed-circuit assembly	W = watt(s)
hd = head	phh = phillips head	w/ = with
hex = hexagon, hexagonal	pnh = pan head	WIV = inverse working volts
hlcl = helical	P/O = part of	ww = wire-wound
Hz = Hertz	pot = potentiometer	
	pozi = Pozidriv	

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Table 6-3. Code List of Manufacturers

The following code numbers are extracted from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, and H4-2, and their supplements.

CODE NO.	MANUFACTURER	ADDRESS
03296	Nylon Molding Corp.	Springfield, NJ
06383	Panduit Corp.	Tinley Park, IL
06540	Anatom Electronic Hardware Div. of Mite	New Haven, CT
09353	C&K Components, Inc.	Newton, MA
23880	Stanford Applied Eng., Inc.	Santa Clara, CA
23936	Pamotor Div., William J. Purdy	Burlingame, CA
28480	Hewlett-Packard Co.	Palo Alto, CA
28875	IMC Magnetics Corp., N.H. Division	Rochester, NH
56289	Sprague Electric Co.	North Adams, MA
71400	Bussman Mfg. Div. of McGraw Edison Co.	St. Louis, MO
71785	TRW Electronic Components, Cinch Div.	Elk Grove Village, IL
75382	Kulka Electric Corp.	Mt. Vernon, NY
94222	Southco, Inc.	Lester, PA